Draft National Strategy on Microelectronics Research (for Public Comment)

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Abbreviations and Acronyms

AFRL Air Force Research Laboratory

AI artificial intelligence

ARL Army Research Laboratory

CMOS complementary metal-oxide-semiconductor

DARPA Defense Advanced Research Projects Agency

DHS Department of Homeland Security

DOC Department of Commerce

DOD Department of Defense

DOE Department of Energy

DOS Department of State

EDA electronic design automation

ESIX Subcommittee on Economic and Security Implications of Quantum Science

FBI Federal Bureau of Investigation

HBCUs historically black colleges and universities

IARPA Intelligence Advanced Research Projects Activity

ICT Information and Computing Technologies

IP intellectual property

MEMS microelectromechanical systems

ML machine learning

MSI minority-serving institution

NASA National Aeronautics and Space Administration

NEC National Economic Council

NIFA National Institute of Food and Agriculture

NIST National Institute of Standards and Technology

NITRD Networking and Information Technology Research and Development

NNI National Nanotechnology Initiative

NRL Naval Research Laboratory

NSA National Security Agency

NSC National Security Council

NSF National Science Foundation

NSTC National Science and Technology Council

ODNI Office of the Director of National Intelligence

OMB Office of Management and Budget

OSTP Office of Science and Technology Policy

PDK process design kit

PPP public-private partnership

R&D research and development

S&T science and technology

STEM science, technology, engineering, and mathematics

USD United States dollars

USDA U.S. Department of Agriculture

USTR U.S. Trade Representative

Introduction

The digital revolution has transformed society. Nearly all aspects of modern life are now dependent on microelectronics,[1] including communications, computing, entertainment, healthcare, energy, and transportation. As a result, microelectronics are essential to the economic and national security of the United States. Rapid innovation in the semiconductor industry has been fueled for decades by research and development (R&D) investments in hardware and software by the Federal Government and the private sector.[2] The intense race to continually increase the performance and functionality of microelectronics, while maintaining or reducing cost and power requirements, has driven the fabrication of ever smaller and more densely integrated components. This miniaturization has required continuous breakthroughs in materials, tools, and design that have ultimately enabled key structures to have dimensions as small as a few atoms in size. The required advances in manufacturing have been enabled by significant investments not only in R&D, but also in developing the manufacturing and metrology equipment and the associated fabrication facilities ("fabs") and packaging facilities required to make advanced integrated circuits and components. The complexity and cost of manufacturing at this scale—establishing a leading-edge silicon fab now costs 10 to 20 billion dollars[3]—has contributed to significant consolidation in the industry. Today, only three corporations in the world are competing to manufacture the latest generations of microelectronics, and no leading-edge (< 10 nm) fab is currently operational in the United States.[4]

In June 2021, the White House released *Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth*, a report on critical supply chains, including the semiconductor manufacturing and advanced packaging supply chain.[5] The report notes that although the U.S. semiconductor industry accounts for nearly half of worldwide revenue, the U.S. share of global semiconductor manufacturing has dropped to an all-time low of 12%, and the U.S. share of packaging has fallen to 3%. As discussed in the report, modern microelectronics manufacturing is an incredibly complex and global process, involving hundreds of steps completed over several months, with many

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[1] Microelectronics in this context refers to integrated electronic devices and systems generally manufactured using semiconductor-based materials and related processing (i.e., in a semiconductor fabrication manufacturing facility, or "fab"). Such devices and systems include analog and digital electronics, power electronics, optics and photonics, and micromechanics for memory, processing, sensing, and communications applications.

[2] The semiconductor industry refers to the manufacturing sector that produces products consisting of semiconductor-based electronic devices and integrated circuits, including advanced packaging and power electronics.

[3] For example, see, *TSMC looks to double down on U.S. chip factories as talks in Europe falter*, www.globalbankingandfinance.com/exclusive-tsmc-looks-to-double-down-on-u-s-chip-factories-as-talks-in-europe-falter; and *Intel: Upcoming U.S. Fab Will Be a Small City, to Cost $60 to $120 Billion,* www.tomshardware.com/news/intel-to-spend-up-to-120-billion-on-new-us-manufacturing-hub.

[4] *See, The Semiconductor Supply Chain: Assessing National Competitiveness* https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief.pdf

[5] *Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth*, The White House, 2021, www.whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf. Note: This initial report did not include power electronics or other specialized semiconductors for clean energy applications such as photovoltaics (PVs), which are expected to be addressed in a follow-on report.

components using international expertise and facilities as they crisscross the world several times. The report concluded that the public and private sectors need to act to increase domestic manufacturing capacity for critical goods, recruit and train a domestic workforce, invest in R&D, and work with America's allies and partners to collectively strengthen supply chain resilience.

The White House supply chain report emphasizes the importance of the semiconductor industry to the U.S. economy, which ranked fourth overall in U.S. exports sales in 2020. The federal government is also an important consumer of microelectronics, and it is critical that it has access to trusted and assured microelectronics for essential functions such as communications, navigation, sensing, critical infrastructure, public health, and national security. Microelectronics underpin a wide range of emerging technologies including quantum information sciences, artificial intelligence, advanced wireless networks (5G and beyond), and clean-energy and energy-efficient technologies needed to address the climate crisis.[6]

The importance of this industry to the Nation's economy and security is evident through the passing of the CHIPS Act of 2022, part of the CHIPS and Science Act of 2022,[7] which appropriated more than $52 billion to grow the Nation's semiconductor manufacturing base and accelerate microelectronics R&D. Moreover, several recent reports emphasized the importance of the industry. For example, in a 2018 assessment, the DOD identified threats to the microelectronics supply chain as well as related R&D and manufacturing issues for multiple critical defense sectors.[8] In 2020, the Congressional Research Service (CRS) examined the technical challenges facing the semiconductor industry, domestic and global supply chains, secure and trusted production of semiconductors for national security, and associated Federal policies and research investments, along with possible legislation to address these challenges.[9] Microelectronics were also called out in 2021 as a key area in the Final Report of the National Security Commission on Artificial Intelligence.[10]

Microelectronics R&D is essential to continued advances in technology and systems, and to the long-term goal of strengthening domestic manufacturing and mitigating supply chain risks. Considering this and these reports, along with Federal Requests for Information (RFIs),[11] unsolicited recommendations

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[6] *Climate change widespread, rapid, and intensifying – IPCC*, https://www.ipcc.ch/2021/08/09/ar6-wg1-20210809-pr

[7] CHIPS Act of 2022 (Division A of Public Law 117-167). https://www.congress.gov/bill/117th-congress/house-bill/4346/text: https://www.congress.gov/bill/117th-congress/house-bill/4346.

[8] *Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States*, DOD, 2018, media.defense.gov/2018/oct/05/2002048904/-1/-1/1/assessing-and-strengthening-the-manufacturing-and%20defense-industrial-base-and-supply-chain-resiliency.pdf.

[9] *Semiconductors: U.S. Industry, Global Competition, and Federal Policy*, Congressional Research Service, 2020, https://crsreports.congress.gov/product/pdf/R/R46581.

[10] *Final Report*, National Security Commission on Artificial Intelligence, 2021, www.nscai.gov/wp-content/uploads/2021/03/Full-Report-Digital-1.pdf.

[11] Relevant RFIs include *Current and Future Workforce Needs to Support a Strong Domestic Semiconductor Industry*, NIST, DOC, 2018, www.federalregister.gov/documents/2018/07/16/2018-15077/current-and-future-workforce-needs-to-support-a-strong-domestic-semiconductor-industry; *National Nanotechnology Initiative Strategic Planning*, OSTP, 2020, www.federalregister.gov/documents/2020/10/13/2020-22556/request-for-information-national-nanotechnology-initiative-strategic-planning; *Microelectronics R&D Facility Capabilities for Prototyping,* DOD, 2020, sam.gov/opp/eaf0eb36b54542b28c6ee88252e9f4b0/view; and *Basic Research Initiative for Microelectronics*, Office of

from the stakeholder community, and multiple reports from the public and private sectors focused on the urgent need to prioritize microelectronics R&D,[12,13] it is clear that a strong, innovative domestic R&D effort is vital. Taken all together, a set of key R&D trends and opportunities emerge from these resources:

- **The diversity of devices and their applications continues to grow beyond conventional processors and memory**, requiring discovery and innovation across a broad front that covers the generation, communication, and processing of data across many scales and types of information systems.
- **A comprehensive approach to R&D across the "full stack" provides an opportunity to achieve performance, reliability, and security improvements in devices and systems**.[14] Although much attention is focused on the design and scaling of foundational devices, there are also major challenges ahead for fabrication, metrology, testing, and advanced packaging. Moreover, challenges are not limited to hardware; innovations in devices, manufacturing, circuits, and systems integration require concomitant innovations across the computer architecture, software, and application layers.
- **Integrated design offers an approach to accelerate innovation**. In addition, it can ensure that critical system attributes are designed in from the start and considered throughout the development cycle, including performance, reliability, energy efficiency, and security.
- **The U.S. microelectronics research ecosystem continues to excel at basic and early stage applied research**, but additional investment in domestic infrastructure and an agile workforce are needed to efficiently transition innovations to industry.
- **Affordable and rapid access to design and prototyping capabilities will increasingly enable domestic innovations to transition more rapidly** from R&D into manufacturing. Capabilities are needed from the device scale to the wafer scale and near or at leading-edge process nodes. Students and researchers need access to these capabilities for experiential workforce training.
- **Access to well-prepared talent is a significant challenge across the entire value chain** and will require both short-term and long-term solutions. Welcoming pathways are needed to make the United States a magnet for outstanding foreign talent in high-demand fields. Improvements in both curriculum and outreach are needed for the equitable and inclusive development of a diverse domestic science, technology, engineering, and mathematics (STEM) talent pool.

Science, DOE, 2019, https://www.federalregister.gov/documents/2019/07/12/2019-14869/request-for-information-basic-research-initiative-for-microelectronics.

[12] Public sector reports include *Basic Research Needs for Microelectronics,* DOE, 2018, www.osti.gov/biblio/1545772; *Semiconductor Foundry Access by U.S. Academic Researchers in Micro- and Nano- Circuits and Systems*, NSF, 2021, nsfedaworkshop.nd.edu/assets/429148/nsf20_foundry_meeting_report.pdf; and Report of the first DOE\AMO Workshop on Semiconductor RDD&D for Energy Efficiency, DOE, 2021, www.energy.gov/eere/amo/articles/amo-semiconductor-workshop-integrated-sensor-systems-report. In addition, summaries of AMO workshop 2 and 3 reports are available at yesevents.com/AMO_Semiconductors and full reports will be posted there in January 2022.

[13] Private sector reports include, for example, *Semiconductor Research Opportunities: An Industry Vision and Guide*, Semiconductor Industry Association (SIA), 2017, www.semiconductors.org/wp-content/uploads/2018/06/SIA-SRC-Vision-Report-3.30.17.pdf; *Chipping In:,* SIA, 2021, https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf; *The Decadal Plan for Semiconductors*, Semiconductor Research Corporation, 2021, www.src.org/about/decadal-plan and *An Analysis of the North American Semiconductor and Advanced Packaging Ecosystem,* IPC, Nov 10, 2021 https://emails.ipc.org/links/IPCadvpack-ecosystem-report-final.pdf.

[14] The term *full stack* captures all the elements of a microelectronics system, from the most basic levels of hardware to the high-level software used by applications programmers.

- **Strong engagement with allies and partners is required to ensure the success of the entire innovation ecosystem**. The semiconductor industry is global; no nation can bring together the technology, supply chains, and expertise to support leading-edge R&D and manufacturing on its own.
- **Improving the energy efficiency of microelectronics is increasingly essential for sustainability**. Rapid growth in microelectronics use and the simultaneous slowing of energy efficiency improvements are creating new economic and environmental risk. Microelectronics R&D investments must include a focus on energy efficiency and reduce the use of materials hazardous to the environment, to reduce this risk.
- **Safeguarding intellectual property is essential to ensure that U.S. industry captures economic benefit to sustain private R&D investments.** Key intellectual property developed by and within the United States must be appropriately protected. Applied research is ultimately intended to provide technical discriminators giving microelectronics manufacturers a strategic advantage in the marketplace. Safeguards (i.e., cybersecurity, etc.) must be implemented to ensure that key innovations are not inappropriately disseminated.

These trends and opportunities have informed the goals and strategic objectives presented in this document to accelerate the pace of innovation and translation through collaborative research, access to advanced infrastructure, and a culture of co-design across the microelectronics R&D enterprise. Attention must focus on developing and sustaining a vibrant and connected microelectronics ecosystem to ensure U.S. leadership in this important area.

The Microelectronics Innovation Ecosystem

The microelectronics innovation ecosystem is complex and extremely capital-intensive, knowledge-intensive, and R&D-intensive.[15] Industry consolidation has imposed limits on the associated R&D ecosystem. With worldwide manufacturing of leading-edge microelectronics now dependent on only a handful of fabs, the opportunity for researchers to exploit advanced processes is limited. Researchers in academia, government, and industry who do not require high-volume production have limited access to the capabilities needed for advancing the R&D frontier, significantly constraining their ability to develop and transition innovations to leading-edge manufacturing. Limited access to leading-edge capability also impacts opportunities to provide the experiential training needed for workforce development.

Beyond the leading edge of current complementary metal-oxide-semiconductor (CMOS) technology, the microelectronics industry is facing profound changes associated with the accelerated pace of innovation and an explosion in the diversity of technologies occurring in academia, national laboratories, government facilities, and companies small and large. Effective pathways for transitioning

[15] For example, see *Measuring distortions in international markets: The semiconductor value chain,* OECD, 2019, www.oecd-ilibrary.org/trade/measuring-distortions-in-international-markets_8fe4491d-en; and *Strengthening the Global Semiconductor Supply Chain in an Uncertain Era*, Boston Consulting Group and the Semiconductor Industry Association, 2021, www.semiconductors.org/strengthening-the-global-semiconductor-supply-chain-in-an-uncertain-era.

new discoveries into applications need to be established and strengthened to ensure that the United States captures the benefits from R&D investments and that key intellectual property (IP) is available for domestic manufacturing. Additionally, as new challenges are identified in manufacturing, these technical needs must be communicated back to the research community.

As part of the national R&D ecosystem, over twenty Federal agencies fund R&D, with the character of the activities determined by the mission of each agency.[16] DOC/NIST, DOD, DOE, NASA, NSF, DHS, and other Federal agencies support both intramural R&D, conducted at government facilities and DOE National Laboratories, and extramural R&D, conducted by academia and industry through grants and contracts. Although much Federal research funding supports fundamental research, the wide span of R&D activities requires protecting the IP developed and securing R&D from unintentional technology transfer. Agencies also support workforce development across all educational levels through a variety of mechanisms, including support for formal and informal learning, internships, and fellowships; curriculum development; and coordinated efforts to broaden participation in STEM. While each agency has mission-oriented priorities determining the focus of its microelectronics-related research,[17] as discussed below and throughout this strategy, there are multiple interagency mechanisms through which R&D priorities and programs are coordinated and the outcomes of research shared for mutual benefit.

Within the microelectronics innovation ecosystem, an important element of Federal funding is support for the infrastructure along the technology development pathway. For early-stage research, many facilities exist in academic institutions, government facilities, and national laboratories, particularly for the fabrication and characterization of materials and devices. Another area of Federal investment is in cyber infrastructure, including modeling, simulation, and data. Many of these user facilities are part of networks connected to the National Nanotechnology Initiative (NNI).[18] These user facilities provide researchers from academia, industry, and government access to suites of tools and scientific expertise that support microelectronics R&D. These facilities have vastly broadened participation of researchers from small businesses and institutions that would not be able to purchase the equipment on their own. This has helped democratize innovation that requires specialized facilities and equipment, especially for semiconductor R&D and fabrication.

Once proofs of concepts at the device level are achieved, innovation often becomes hindered in the current U.S. ecosystem by a lack of access to the necessary advanced development capabilities. Investments in domestic design, fabrication, and packaging capabilities, as part of the CHIPS Act of 2022, will help address this “lab-to-fab” gap. These investments are intended to enable and sustain advanced prototyping and scale-up of new devices and architectures, along with the associated manufacturing and metrology instrumentation, and in concert with the required design of software and

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[16] *Research and Development in the President’s FY 2022 Budget Request* https://www.whitehouse.gov/wp-content/uploads/2021/05/ap_14_research_fy22.pdf.

[17] See the Appendix for summaries of each agency’s activities related to this plan.

[18] www.nano.gov/userfacilities.

applications. Moreover, access to these capabilities by both researchers and students will provide the hands-on, experiential training needed to expand the domestic microelectronics workforce.

The CHIPS for America Act of 2021[19] authorized multiple programs to help bridge this lab-to-fab gap, while the CHIPS Act of 2022 appropriates the funding for the programs (for simplicity, the two acts will be collectively referred to here as the "CHIPS Acts"). Section 9906, of the CHIPS for America Act of 2021, directs the DOC to establish a National Semiconductor Technology Center to conduct research and prototyping of advanced semiconductor technologies; a microelectronics research program at NIST to conduct semiconductor metrology research and development; a National Advanced Packaging Manufacturing Program to strengthen semiconductor advanced test, assembly, and packaging capability; and up to three Manufacturing USA Institutes focused on semiconductor manufacturing. Section 9903, of the same law, authorizes DOD to establish a National Network for Microelectronics Research and Development to enable the laboratory-to-fabrication transition of microelectronics innovations in the United States.

Within the broader U.S. R&D ecosystem, there are many regional innovation hubs around the country composed of industry clusters complemented by Federally supported academic centers, often focused on specific technologies and/or local research strengths. These local hubs are a valuable national resource and ensuring that they are well coupled to other elements of the overall R&D ecosystem, including microelectronics, will strengthen the national innovation base.

The U.S. semiconductor industry invests heavily in R&D efforts, estimated to be $44 billion in 2020.[20] To maintain their world-leading expenditures on R&D, U.S. companies must have access to foreign markets where they can compete and win based on superior technology. Trade and national security policies must protect U.S. companies from discrimination in global markets. In efforts to protect technology, collaboration and alignment with allies and partners will not only provide security more effectively, but will also help U.S. companies hold their ground in the global competition for technology leadership.

A Whole of Government Approach

Recognizing the critical role of microelectronics to our health, environment, economy, and national security, a whole-of-government effort is underway to sustain and advance global leadership by the United States and its allies in this important field. U.S. agencies are using their respective authorities to advance R&D and promote policies to support U.S. industry, protect intellectual property and national interests, and ensure domestic access to secure microelectronics. The Federal Government is engaging and collaborating with allies and partners to strengthen the global microelectronics innovation ecosystem and secure supply chains. Agencies are also supporting and collaborating on activities to improve STEM education and increase participation in STEM careers, and to train and expand the microelectronics workforce at all levels including advanced degrees. Coordinated through the White

[19] William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021, (Public Law 116-283), Title XCIX ("Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America") (herein "CHIPS for America Act of 2021").

[20] SIA, 2021 State of the Industry Report, 2021; 2021-SIA-State-of-the-Industry-Report.pdf (semiconductors.org).

House, these efforts will not only fuel new discoveries to drive microelectronics innovation but will also help these discoveries transition to manufacturing and provide good-paying jobs to people from across all of America.

The White House and Federal departments and agencies will work together and with academia, industry, non-profits, and international allies and partners over the next five years to fuel discoveries for future generations of microelectronics; expand, train, and support a diverse workforce; and facilitate the rapid transition of R&D to industry.[21,22]

The White House and Federal departments and agencies recognize that openness is a foundation for R&D leadership and that international talent flow is critical to the success of the global enterprise.[23,24] However, as made clear in Guidance for Implementing National Security Presidential Memorandum 33 (NSPM-33),[25] the U.S. Government and its partners must strengthen protections of R&D against foreign government interference and exploitation, diligently safeguarding intellectual capital and property. Protections may include improved, risk-based processes for evaluating research partnerships and proposed foreign investments; active participation of U.S. experts in international standards organizations; closer coordination with international partners on research security; and a campaign of outreach and education on the importance of this topic across the microelectronics R&D community.

[21] OSTP, as directed in the CHIPS for America Act of 2021, established the NSTC Subcommittee on Microelectronics Leadership (SML) to identify priorities, coordinate interagency research and development (R&D) efforts, and develop this National Microelectronics Research Strategy.

[22] Many aspects of microelectronics R&D intersect with other initiatives and Biden-Harris Administration priorities, including the National Nanotechnology Initiative, the Future Advanced Computing Ecosystem (formerly the National Strategic Computing Initiative), the National Quantum Initiative, and the Networking and Information Technology Research and Development (NITRD) Program. The SML is working with all of these efforts to ensure synergy and coordination.

[23] https://www.quantum.gov/wp-content/uploads/2021/10/2021_NSTC_ESIX_INTL_TALENT_QIS.pdf

[24] https://www.whitehouse.gov/briefing-room/statements-releases/2022/01/21/fact-sheet-biden-harris-administration-actions-to-attract-stem-talent-and-strengthen-our-economy-and-competitiveness/.

[25] *Guidance For Implementing National Security Presidential Memorandum 33 (NSPM-33) On National Security Strategy For United States Government-Supported Research And Development,* https://www.whitehouse.gov/wp-content/uploads/2022/01/010422-NSPM-33-Implementation-Guidance.pdf

Goal 1. Fuel Discoveries for Future Generations of Microelectronics

R&D supported by the Federal Government has been instrumental in laying the foundation for advances in microelectronics and in educating the research and skilled technical workforce needed for design, manufacturing, and application development. The increasing diversity of microelectronics technology and pace of innovation, combined with the growing risks to the global manufacturing and supply chain, requires a renewed Federal focus on R&D investment in ways that will alter these trajectories and ensure the future health, economy, and national security of the Nation. Success requires strategies that engage all sectors of the R&D ecosystem and leverage education, workforce, manufacturing, trade, and regional economic development policies. Federal agencies, in collaboration with industry, academia, and partners and allies must work together to accelerate the pace of innovation and translation through collaborative research, access to advanced infrastructure, and a culture of co-design across the microelectronics R&D enterprise.

The past six decades have seen incredible progress in computational power and energy efficiency enabled, in part, by continued miniaturization (supported by concomitant advances in materials, design, metrology, and manufacturing). However, this trend in transistor scaling cannot continue indefinitely as the smallest device feature sizes approach the atomic scale. Furthermore, there are emerging applications that will require heterogeneous devices and materials. The semiconductor industry has therefore entered a period of rapid and profound change, and one in which performance advances can no longer be sustained solely by continued miniaturization of silicon-based devices.

For example:

- The *explosion of data* and the *emergence of artificial intelligence* enabled by machine learning (ML) is driving the development of novel "compute-in-memory" architectures that promise to overcome the "von Neumann bottleneck"—the energy inefficiency and high latency caused by shuttling data back and forth between separate memory and compute elements.
- As intrachip and interchip data rates have increased, *photonic interconnects*, previously only used in long-haul links over optical fiber, are being *integrated with electronics* in advanced packaging to move data efficiently.
- *Advanced photonics* is poised to deliver dedicated ML/artificial intelligence (AI) hardware that operates at *low power* and extraordinary speed.
- A revolution is underway in *electronic design automation (EDA*) that will make it feasible to design custom circuits optimized for almost every conceivable application. These custom circuits will deliver tremendous gains in speed and efficiency and affect the performance of every information technology sector, from data centers to edge computing and the internet of things (IoT).
- *Heterogeneous and domain-specific computing architectures* that optimize performance for specific applications are being deployed to accelerate time-to-solution.
- Progress is being made *integrating semiconductor systems with biomolecular, biological, and bio-inspired systems* that may one day deliver ultra-energy efficiency and other unique capabilities in computation, AI, robotics, sensing, and healthcare beyond the potential of either system on its own.
- As electronics move towards more *heterogeneous architectures*, performance metrics become more complex. Heterogeneous integration—the science and technology of bringing disparate materials, devices, and circuits together to create highly functional, high-performance systems—is key to enabling continued progress. However, as more and more diverse

components are integrated, the physical, electronic, optical, and software challenges of making them operate seamlessly together become more complex.

As referenced in the introduction, there are calls to not only support the underlying science that shapes and drives microelectronics, including computer science, computing architectures, physics, chemistry, and materials science, but also to widely embrace the principles of integrated design where these different aspects of research inform and guide each other synergistically, and with sustainable development in mind. Open communication between all levels of the stack is essential to ensure that end-use requirements inform research, and research breakthroughs are rapidly incorporated into development efforts. Such an integrated approach is the only way to guarantee that critical system attributes, such as security, reliability, and radiation-hardness,[26] are designed in from the start and considered throughout the development cycle.

Strategic Objective 1.1. Support the development of advanced materials, devices, components, interconnects, and circuits with an emphasis on systems-level integrated design and coordination with industry.

U.S. industry leadership in microelectronics must overcome significant challenges in device physics and fabrication. Deep innovation is therefore needed to identify and transition novel materials and devices from lab-to-fab to enable continued advances in functionality and performance. Satisfying the continually increasing demand for bandwidth and processing power for information and computing technologies (ICT) systems, along with the expected growth in the spectrum of applications, requires discovery and development from devices to systems. Central to this strategy is the need for access to design and fabrication facilities, including those equipped to incorporate unconventional materials and/or processes, often in heterogeneous combination with Si-CMOS technologies. Innovations across all levels of the computing stack need to be fully exploited to enable further progress with complex scalable designs in leading-edge Si-CMOS.

Advances in characterization tools and techniques will also be needed to enable detailed and comprehensive investigations of new materials and designs and to do so with unprecedented spatial resolution, sensitivity, and bandwidth. The increasing complexity of circuits and systems, including those operating with signals in and interacting across multiple physical domains, will require complementary, multimodal metrology tools to measure performance and provide the data necessary to validate the models that, for example, support Electronic Design Automation (EDA).

In addition to coordination across the hardware-software stack, coordination is required across the R&D community to achieve the best outcomes through synergistic flow of research results. University and small-business researchers must have access to design tools, fabrication facilities, and related infrastructure in which to test their ideas. Commercial fabrication facilities will benefit from working with early-stage testers of novel technology approaches. Likewise, industry R&D will benefit from the training of an advanced research workforce skilled in these areas and graduating from U.S. universities

[26] Some space, energy, and defense applications require electronics that must function when subjected to a range of radiation sources, including cosmic rays. Radiation-hardened microelectronics perform critical sensing and computational functions so that these devices work as intended.

to join their corporate R&D efforts. An important aspect of this collaboration must be to establish and maintain effective research security measures to prevent R&D activities from creating unintended technology transfer.

Key Strategy 1.1.1: Accelerate the discovery and development of materials that provide new capabilities or functional enhancements.

Materials R&D is central to meeting emerging needs across all sectors and application areas. Materials are needed to address energy efficiency, information speed and bandwidth, novel computing architectures, and sustainable development.

Coordination with other entities in the semiconductor materials and associated research ecosystem, including private sector companies and consortia, will provide a pathway to deployment of advanced materials for devices, interconnects, circuits, and systems. Frameworks like the Materials Innovation Infrastructure developed as part of the Materials Genome Initiative[27] can play an important role in organizing the materials community around grand challenges in developing new capabilities or functional enhancements for microelectronics.

Elements of advanced materials R&D to support new capabilities include:

- Focused research on emerging materials including two-dimensional (2D) materials and designs exploiting quantum effects, materials for energy-efficient electronics, materials for use in extreme environments, materials optimized for high-bandwidth interconnects (both optical and electrical), and biotic-abiotic hybrid systems.
- Unified semiconductor materials data infrastructure to facilitate knowledge sharing and accelerate innovation.
- R&D efforts to develop manufacturing-capable tools and processes for new and emerging materials.
- Research to improve sustainability in processing, fabrication, and supply chains from discovery and throughout development and the full lifecycle, including more eco-friendly materials and wider use of earth-abundant elements that reduce supply-chain vulnerabilities.
- Access to fabrication facilities equipped to incorporate unconventional materials and/or processes, possibly in heterogeneous combination with Si-CMOS technologies.

Key Strategy 1.1.2: Increase the accessibility of circuit design, simulation, and emulation tools.

Circuit design, simulation, and emulation tools applicable to new materials, devices, circuits, and architectures are essential to continued innovation and device scaling. However, complexity and cost have increased significantly over the past several decades to the point where access to these critical tools by start-ups and small businesses is limiting the realization of new custom computing processors and computing architectures.

Strategic approaches to improve access include efforts to:

[27] NSTC Materials Genome Initiative Strategic Plan, 2021, https://www.mgi.gov/sites/default/files/documents/MGI-2021-Strategic-Plan.pdf.

- Create and develop accessible tools that can facilitate the design, modeling, simulation, and exploration of new forms of computing architectures and computing processors (while respecting IP, export controls, and other legal and regulatory boundaries).
- Facilitate the utilization of and access to high-performance computing resources required for modeling and simulation needed to support the evaluation of processor performance prior to incurring prototyping costs.
- Further the integration of AI and machine learning in EDA tools to support the design and development of innovative circuit and system architectures.[28]
- Advance the development of formal and end-to-end validation methods, which includes appropriate materials data and input information, to overcome bottlenecks in circuit and system design and simulation to manage increasingly complex and heterogeneous systems.

Key Strategy 1.1.3: Develop a diverse array of robust processing architectures and associated hardware needed for future systems.

The rapid growth and utilization of advanced computing resources have created performance and energy demands that are pushing the boundaries of state-of-the-art Si-CMOS designs. Non-von Neumann computing architectures, such as neuromorphic, deep learning, analog, quantum, and asynchronous computing, will be increasingly useful in a wide range of commercial and national security applications. Making the most of this new diverse array of processing architectures requires innovations across the entire stack.

Key research and development needs include:

- Increased understanding of the *algorithms, programming models, and compilers* required for optimal performance of these architectures.
- *Manufacturing and design capabilities* optimized for the production of these novel processing architectures.
- Development of novel architectures in addition to *new integrated circuit designs* that enable the optimal integration of non-von Neumann components with traditional computing architectures.
- *Quantum information science research*, including quantum computing, quantum networking, and quantum sensing, which will demand a wide range of new systems design approaches in addition to advanced fabrication capabilities and exotic materials.[29]

Key Strategy 1.1.4: Develop processes and metrology for heterogeneous integration.

Heterogeneous integration, which refers to the integration of several distinct technologies that are themselves the result of integrating multiple systems, will be a critical driver of future innovation in microelectronics. Examples can include integration on single chips, multiple chips, or chiplets on substrates. Success in heterogeneous integration leads to better yields, lower costs, greater functionality, reuse of IP enabling accelerated design iterations and customization, and improved energy efficiency. Integration is critical across an application space that ranges from high-performance

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[28] *NSF Workshop on Micro/Nano Circuits and Systems Design and Design Automation: Challenges and Opportunities*, University of Notre Dame, 2021, nsfedaworkshop.nd.edu/assets/432289/nsf20_eda_workshop_report.pdf.

[29] Coordinated under the National Quantum Initiative, see www.quantum.gov.

computing to healthcare to positioning, navigation, and timing. Heterogeneous integration and the advanced packaging technologies that make it possible are growing twice as fast as traditional packaging.[5] This growth presents the United States with a rare opportunity to establish a lead in a critical area, despite the dominance of overseas assembly and test facilities in conventional packaging.

Successfully capturing the advantages of heterogeneous integration will require addressing many competing research challenges, including materials, energy, cost, yield, and validated modeling.

Key research challenges include:

- The development of new materials for substrates and encapsulation/molding to expand the available design space, and for which collaboration and partnerships with materials suppliers will be essential.
- Robotic systems needed to achieve comprehensive automation in semiconductor manufacturing and assembly.
- Innovative interconnect technologies to increase energy efficiency and density.
- New, high-speed methods to inspect components prior to assembly and to monitor interfaces during assembly to reduce defective components or defects in interfaces between components.
- Enhanced tool metrology and inspection capabilities, including novel optical sources and high-speed detectors over wavelengths from the infrared to the x-ray.
- Application of AI and ML approaches to address the challenges associated with the expected high data rates and large data volumes generated as a result of heterogeneously integrated logic devices.
- Improved physics-based modeling of the thermal, mechanical, and electromagnetic behavior of the complete system and development of new, high-resolution methods to measure these behaviors to validate model accuracy and system performance.
- Integrated design tools and methods to ensure that circuits, architectures, and packages are designed together to maximize system performance.

Key Strategy 1.1.5: Prioritize hardware integrity and security as an element in co-design strategies across the stack.

In the face of threats from nation-state and criminal adversaries, the potential for the insertion of malicious alterations into components ranging from circuits to software combined with the need to prepare for a post-quantum-computing world make it essential that integrity and cybersecurity be a foundational component of system design.[30,31] Co-design of hardware with software is needed to meet this challenge in a way that provides maximum protection while minimizing the impact on system performance.[32] The design process must allow for iteration between hardware, software, and security constraints. To meet economic and national security needs, security must be incorporated in co-design R&D as a design constraint at the same level as performance.

[30] Cybersecurity R&D challenges and goals for hardware and software are described in NITRD's *Federal Cybersecurity Research and Development Strategic Plan* , https://www.nitrd.gov/pubs/Federal-Cybersecurity-RD-Strategic-Plan-2019.pdf.

[31] https://www.whitehouse.gov/briefing-room/statements-releases/2022/05/04/national-security-memorandum-on-promoting-united-states-leadership-in-quantum-computing-while-mitigating-risks-to-vulnerable-cryptographic-systems/

[32] See, for example, D. Dangwai et al., *SoK: Opportunities for Software-Hardware-Security Codesign for Next Generation Secure Computing*, arxiv.org/abs/2105.00378.

Research needs to improve hardware integrity and security include:

- The development of accurate threat models to support the analysis of the cost-benefit tradeoffs of different security approaches.
- The creation of high-level conceptual models of integrity and security (analogous to abstraction layers in computer science) to help the various disciplines in the co-design community communicate and collaborate more effectively.
- New automation and support structures to enable applications to be built on secure systems and to support the universal adoption of new applications.
- The establishment of co-design centers of excellence, in which security is a primary design constraint within each of the hardware focus areas.

Key Strategy 1.1.6: Invest in R&D for manufacturing tools and processes needed to support transition of innovations into production-worthy fabrication processes.

While important manufacturing technology advances will continue at micrometer scales, much that is cutting edge is already and will continue to be at the nanometer scale—even at the atomic scale for some features. To meet the demand for enhanced device performance and energy efficiency, the corresponding development of manufacturing processes, tools, and metrology with unprecedented precision is required. So-called "ultra-precision manufacturing" (UPM) is the next step in a long history of manufacturing at ever-smaller scales.[33] The need for ultra-precision also presents an opportunity to take advantage of material properties that are unique to the nanometer scale, such as tunneling or magnetic and spin interactions, to realize powerful new functionalities. Novel fabrication methods will be effective only if they can be scaled to achieve commercial volumes. Advanced manufacturing R&D to scale up manufacturing-scale processes and tools is therefore essential.[34]

Key R&D needs for UPM tools and processes include:

- The development of *ultra-precision characterization, advanced lithography, and metrology tools and improved quality control*, including accurate reference structures at the sub-10 nm scale.
- *Improvements in processes* such as atomic-layer deposition and etching to support reduced feature sizes and more complex device geometries.
- *High-throughput experimentation and modelling methods*, coupled with new capabilities in *optical, electron, and scanning probe microscopy inspection tools* to improve speed, throughput, yield, precision, and accuracy.
- The development of *hybrid metrology methods* that combine data from multiple measurement tools integrated with new ML methods to utilize the data and enable process optimization.
- Further development and use of *in situ* metrology to accelerate the integration of real-time process control and reduce process variability—a key driver of costly *ex situ* metrology. Progress in this area requires advances in the integration of multimodal measurements, software integration, and tool development.

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[33] See for example, N. Taniguchi, Current status in, and future trends of, ultraprecision machining and ultrafine materials processing, *CIRP Annals*, 32(2) (1983): 573–582, doi.org/10.1016/S0007-8506(07)60185-1.

[34] DOE Workshop report on Ultra-precise control for ultra-efficient devices: https://www.energy.gov/sites/default/files/2022-02/AMO%20Semiconductor%20Workshop%20II%20Report%20FINAL_compliant_02-08-2022.pdf

Strategic Objective 1.2. Support and expand access to R&D infrastructure

The semiconductor R&D infrastructure exists across a continuum, supporting activities ranging from the exploration of new materials to the implementation of new system architectures. The incredible complexity of modern semiconductor and microelectronic systems is best managed by enabling each level in the stack to judiciously abstract and inform the key features of neighboring levels as part of a co-design approach with bidirectional information flows. Material characteristics are abstracted into device models, device behaviors are incorporated into circuit models, circuits into architectures, and so on all the way up to applications. Likewise, application and software characteristics inform architectures, which guide circuits and so on down the stack.

As the R&D focus moves up the stack, the infrastructure must be aligned to assure a continuous path for scientific and technological developments made at each level to inform those at the next, and ultimately to feed into commercial design and manufacturing. At the lowest level of the stack, maximum flexibility is required of facilities to accelerate the discovery of new materials that will enable breakthrough performance. As these materials are identified, they must be made available to the research community to integrate into devices to determine whether the anticipated performance benefits can be realized. Further up the stack, facility flexibility is less important compared to the existence of reliable and robust fabrication processes that enable repeatable and reliable measurements of device performance. At the circuit level, access to documented and supported process design kit (PDK) modules is essential. Creating such a full-spectrum R&D ecosystem will require supporting and expanding access to the infrastructure needed for innovation. This infrastructure comprises three critical components: the hardware and software tools, the data and data sharing infrastructure, and the expertise to make the best use of the tools and data. Ready access to these tools and data is also an essential prerequisite for training and maintaining the expertise of the research and manufacturing workforce.

The infrastructure needed to support the R&D continuum ranges from facilities for the early-stage development of materials, structures, devices, fabrication processes, and metrology and characterization tools, to access to leading-edge prototyping facilities using standardized processes. The CHIPS Acts investments are intended to bridge the gap between early-stage R&D and prototype, enabling limited experimentation with new materials, processes, and metrology. (Early-stage research facilities are addressed here, with leading-edge prototyping facilities addressed under Goal 3.)

Key Strategy 1.2.1: Support networks of device-scale R&D fabrication and characterization user facilities.

The support of new concepts for electronic, photonic, and micromechanical devices that advance both “More-Moore” and “More-Than-Moore” solutions[35] requires increasingly complex and costly characterization and fabrication tools and facilities. Semiconductor materials synthesis and characterization, and device fabrication and measurement involve multiple, separate steps requiring

[35] More-Moore refers to advances in CMOS transistor scaling, and More-than-Moore refers to incorporating devices with functionality that does not necessarily scale like Moore’s Law, such as radio-frequency, photonic, and MEMS devices.

different tool sets. Researchers working in microelectronics need access to user facilities equipped with complete suites of fabrication and characterization tools that require constant capital investments to remain current. In addition to the instrumentation, effective user facilities require expert staff to train new users, which helps lower the barrier to access and provides an important role in education and workforce development.

Fortunately, the microelectronics R&D community can build upon the foundation of user facilities established as part of the NNI.[36] These facilities, along with other major university centers and National Laboratories, provide access to a broad suite of tools at the materials and device levels. As discussed in Strategic Objective 3.2 below, it is critical to build out and connect the necessary infrastructure across the entire research to manufacturing continuum.

Key needs for the R&D fabrication and characterization facilities include:

- A gap analysis of the current facility networks followed by efforts to address capability gaps within existing facilities and establish new capabilities where needed to comprehensively address the needs of different areas and levels in the stack.
- Agreements with allied and partner governments that provide U.S.-based researchers access to cutting-edge manufacturing facilities to bridge current domestic gaps.
- Funding models that enable facilities to acquire sufficient state-of-the-art tools to build critical mass in their focus area(s), support expert facility technical staff to guide and assist users, and afford ongoing recapitalization as needed to maintain both state-of-the-art and state-of-the-practice capabilities.
- Reduced barriers to facility access including through outreach to the research community, affordable access and operating costs, and simple, equitable access models. Improved access through investments in remote access technologies that can further extend the geographic reach of every facility and promote equity of access.
- FAIR (findable, accessible, interoperable, and reusable) data management systems to maximize the access of all users to information generated in the facilities.
- Collaboration mechanisms across departments and agencies to facilitate the transition of work from one facility to the next as users' technologies mature and the capabilities evolve.

Key Strategy 1.2.2: Improve access for the academic and small-business research community to flexible design tools and wafer-scale fabrication resources.

Currently, the costs of design tools, notably PDKs and EDA, combined with the costs of foundry fabrication runs can be prohibitive for academic and small-business research communities. In addition, there is no well-established pathway for a wafer fabricated at a foundry to be further processed in a more flexible research facility. The CHIPS Acts investments will help address this domestic gap between device-scale R&D and advanced prototyping, through investments in infrastructure complemented by new public-private partnerships, including a new system capable of providing efficient, affordable access to a network of shared resources for wafer-scale R&D.

[36] These facilities include the NSF-funded National Nanotechnology Coordinated Infrastructure (NNCI), based in universities across the country, the DOE Nanoscale Science Research Centers, co-located with other facilities in National Laboratories, and the DOC/NIST Center for Nanoscale Science and Technology NanoFab and facilities being set up in support of the National Quantum Initiative, including the DOE National QIS Centers and NSF Q-AMASE program.

Key needs to improve access to design tools and fabrication resources include:

- Flexible models that expand the availability of advanced PDKs, standard cell libraries, and certain IP (i.e. memory controllers, cores, etc.) for domestic researchers while protecting commercial IP and propriety information.
- An expanded range of modules available for EDA tools through the development of specific, targeted process and device modules by researchers in collaboration with industrial partners.
- Broader partnerships with EDA vendors to make design tools available to more university and small-business researchers at significantly reduced cost. The DARPA Toolbox Initiative[37] is one example of a program facilitating access to design tools and proven IP for the R&D community. Where possible, programs should promote the standardization of PDKs used in R&D to increase interoperability across design and manufacturing vendors.
- More multi-project wafer capacity at fabrication facilities to reduce cost and design-test cycle times and to expand access and accelerate innovation.

Key Strategy 1.2.3: Facilitate research access to key functional materials.

The microelectronics industry would not be possible without a supply of ultra-pure and nearly defect-free materials. Development of new electronic, magnetic, and photonic devices is likewise dependent upon the supply of appropriate functional materials. Several of these materials are of intense interest to the R&D community and are being actively developed at the device, circuit, and system level in applications ranging from machine learning accelerators, to quantum networks. These materials include III-V semiconductors (as well as quantum dot and quantum well materials made from them), thin-film lithium niobate, silicon carbide on insulator, diamond, and a host of multiferroics. However, many of these materials are only available from overseas suppliers. Other materials can be obtained domestically, but often only from a single university laboratory with limited capacity to supply external research groups and sometimes with inconsistent quality.

Strategies to ensure a robust and high-quality domestic supply of functional materials to accelerate the pace of device and integration research include:

- Working with and utilizing U.S.-based materials suppliers to ensure that domestic capacity is maintained and the necessary institutional knowledge and expertise to support manufacturing continues to be developed and captured domestically (and shared with international partners).
- Additional funding and support to U.S.-based research institutions at the forefront of materials development to support the dedicated staff required to expand the capacity to supply domestic researchers (and researchers from international partners) with their novel materials. Focused research grants requiring industrial participation could be used to build collaborations to develop the materials supply and transfer research expertise to the commercial sector.
- Funding opportunities to domestic material suppliers to encourage the development of new material processes and reduce acquisition costs for researchers.

[37] DARPA Toolbox Initiative, www.darpa.mil/work-with-us/darpa-toolbox-initiative.

Goal 2. Expand, Train, and Support the Workforce

U.S. leadership in microelectronics requires a robust domestic workforce. According to the DOL Bureau of Labor Statistics (BLS), semiconductor and other electronic components manufacturing employed 376,000 people in 2020,[38] with the broader sector of computer and electronic product manufacturing employing over 1 million people.[39] An economic analysis commissioned by the semiconductor industry reported that 277,000 people were directly employed by that industry in R&D, design, and manufacturing activities in the United States in 2020, with a total of 1.85 million jobs supported overall.[40] This report also found that the average pay across the education spectrum for these jobs is notably higher than for other industries, consistent with BLS data showing that workers in the semiconductors and electronic components sector earned nearly 50% more than the average private-sector employee.[41]

The semiconductor industry workforce is concentrated in a few regions of the country.[42] High demand STEM occupations in the industry are dominated by engineering and computer software development and generally require a bachelor's or advanced degree for employment. Competition for degreed professionals is increasingly at a premium, especially at the PhD level. Industry hiring for PhDs in computer and information science and in mathematics has exploded during the period 2010-2019, with company hires of PhD computer and information scientists increasing by 103% and company hires of PhD mathematical scientists expanding by 160% during that period.[43] Within the manufacturing workforce, less than a third of employees have a bachelor's or graduate degree, but an associate degree is now typically required at a minimum. Foreign-born scientists and engineers make up 41% of the high-skilled technical workers in the semiconductor and other electronic components manufacturing sector.[44] This is consistent with data showing that foreign-born persons constitute 30% of workers in all science and engineering occupations and hold more than half the doctorates in engineering, computer science, and mathematics occupations.[45] Foreign students who complete graduate education in STEM in the United States have relatively few predictable options to secure permanent status, and therefore many return to their home countries.[46] In the last decade, a growing fraction of the high-skilled workers educated in the United States have been returning to their home or other countries. Moreover, the number of domestic students entering microelectronics as a career has declined over the past decade.

[38] Annual employment (thousands of jobs) for NAICS 3344, semiconductor and other electronic component manufacturing, U.S. total, 2021, beta.bls.gov/dataViewer/view/timeseries/IPUEN3344__W200000000.

[39] Computer and Electronic Product Manufacturing: NAICS 334, www.bls.gov/iag/tgs/iag334.htm.

[40] Semiconductor Industry Association and Oxford Economics, 2021, *Chipping In, the Positive Impact of the Semiconductor Industry on the American Workforce and How Federal Industry Incentives Will Increase Domestic Jobs*, www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf.

[41] www.bls.gov/web/empsit/ceseeb3a.htm.

[42] Congressional Research Service, 2020, *Semiconductors: U.S. Industry, Global Competition, and Federal Policy,* crsreports.congress.gov/product/pdf/R/R46581/5.

[43] National Science Foundation, 2010 and 2019 National Survey of College Graduates, https://www.nsf.gov/statistics/srvygrads/.

[44] Hunt and Zwentsloot, 2020, *The Chipmakers: U.S. Strengths and Priorities for the High-End Semiconductor Workforce*, cset.georgetown.edu/wp-content/uploads/CSET-The-Chipmakers.pdf.

[45] National Center for Science and Engineering Statistics, 2020, *The State of U.S. Science and Engineering 2020*, ncses.nsf.gov/pubs/nsb20201/u-s-s-e-workforce.

[46] Congressional Research Service, 2022, *U.S. Employment-Based Immigration Policy,* https://crsreports.congress.gov/product/pdf/R/R47164.

A semiconductor industry economic analysis forecasts that an additional $50 billion Federal investment to incentivize domestic manufacturing would create nearly 100,000 direct jobs associated with the manufacturing expansion, including at least 40,000 new, long-term jobs. As discussed above, these jobs are expected to be among the highest-paying in the economy. Meeting this demand will require strategies to develop, attract, and retain a larger pool of talent both domestically and from abroad, ranging from the skilled technical workforce to doctoral-level researchers and educators. Even independent of potential for job growth, the United States will be increasingly competing internationally for talent in this industry, requiring strategies to increase the pool of well-prepared, domestic STEM talent.

Considering the array of public and private-sector reports and stakeholder input reveals several key findings and challenges. Industry competition for highly skilled talent is fierce, compounded by an aging workforce and competition with other technology sectors. U.S. companies are especially challenged to find candidates to fill positions that require advanced degrees and U.S. citizenship. Moreover, the U.S. education system is currently not preparing enough students across all educational and job levels with the knowledge and experiential skills needed for this workforce. Finally, all stakeholders must work together to remove historic and entrenched systemic inequities that prevent some groups from accessing the high-paying jobs in this industry—a requirement for both increasing the domestic talent pool and maximizing innovation through a diverse and inclusive workforce.

Strategic Objective 2.1. Expand the workforce to support growth of the U.S. microelectronics industrial base.

Competition for talent necessitates strategies that will expand the available labor pool, drawing on both domestic and foreign talent across all educational levels, including those currently underrepresented in the STEM workforce. The United States must continue to support K-12 efforts in STEM and inspire the next generation of innovators by engaging students in exciting hands-on projects and in solving real-world problems. Programs and activities should raise awareness of career opportunities early and sustain outreach efforts to attract more domestic talent into electrical engineering, computer science, and mathematics. Early efforts to attract workforce must be paired with subsequent efforts to retain a diverse workforce at all degree levels. As the semiconductor industry continues to innovate and diversify, fields like chemistry, chemical engineering, and materials science and engineering will also be of increasing importance.

As for all fields of STEM, the Nation must double down on efforts to break down barriers that have historically prevented broad segments of society from fully participating in STEM education and careers, assuring that all Americans have lifelong access to high-quality STEM education and that the United States will be the global leader in STEM literacy, innovation, and employment.[47]

[47] Readout of the Third Roundtable in “Time is Now: Advancing Equity in Science and Technology” Series, 2021, www.whitehouse.gov/ostp/news-updates/2021/09/13/readout-of-the-third-roundtable-in-time-is-now-advancing-equity-in-science-and-technology-series-emerging-models-and-pathways-for-success-i-institutional-and-academic-contexts.

Building and retaining the domestic workforce will also require incentives to compete with recruitment efforts by other nations, including preferential immigration for foreign-born, U.S.-educated students with key R&D and manufacturing-related skills.[48] Research protection remains paramount, but such concerns must be balanced against the overwhelmingly positive role international talent has played, and will continue to play, in the U.S. innovation ecosystem.[49]

The rapid pace of semiconductor technology advances requires engineering and science programs to remain current to avoid opening a gap between education and industry needs and imposing a difficult school-to-work transition for graduates. Mitigating these challenges will require additional investments and partnerships with business and industry representatives along with educators at community colleges and universities.

Key needs include:

- Technical and undergraduate curricula with topics such as very large-scale integration (VLSI) design, fabrication and test, and modeling, complemented by the resources to enable large cohorts of students to have immersive laboratory experiences.
- Expanded microelectronics and related education across the country, including efforts targeted at smaller and rural schools, community colleges, and at historically black college and universities (HBCUs) and other minority-serving institutions (MSIs), which may provide access to an underutilized resource for the semiconductor industry.
- Initiation and promotion of specialized graduate-level curricula and MS and PhD programs developed to align with emerging industry needs.
- Mechanisms to more easily recruit and retain foreign students and professionals to meet the workforce demands of the U.S. microelectronics industry.[50]

Strategic Objective 2.2. Provide students with relevant, experiential training.

Responsive education and training systems are needed that can adeptly respond to the acceleration of technology development and innovation.[51] Currently, most U.S. educational institutions do not have the capability and resources to provide hands-on training that fully prepares students for the microelectronics workforce. Community colleges struggle to procure the specialized equipment for

[48] National Science Board, 2022 *International STEM Talent is Crucial for a Robust U.S. Economy*, https://www.nsf.gov/nsb/sei/one-pagers/NSB-International-STEM-Talent-2022.pdf; U.S. Government Accountability Office, July 2022, *Semiconductor Supply Chain: Policy Considerations from Selected Experts for Reducing Risks and Mitigating Shortages*, https://www.gao.gov/assets/gao-22-105923.pdf, Congressional Research Service, 2022, *U.S. Employment-Based Immigration Policy,* https://crsreports.congress.gov/product/pdf/R/R47164, Krol, 2021, *Effects of Immigration on Entrepreneurship and Innovation*, https://www.cato.org/sites/cato.org/files/2021-10/cj-41n3-5.pdf.

[49] Science and Technology Policy Institute, 2021, *Economic Benefits and Losses from Foreign STEM Talent in the United States*, https://www.ida.org/research-and-publications/publications/all/e/ec/economic-benefits-and-losses-from-foreign-stem-talent-in-the-united-states; National Science and Technology Council, Subcommittee on Economic and Security Implications of Quantum Science, 2021, *The Role of International Talent in Quantum Information Science*, https://www.quantum.gov/wp-content/uploads/2021/10/2021_NSTC_ESIX_INTL_TALENT_QIS.pdf.

[50] New STEM Resources Available on USCIS Website, 2022,https://www.uscis.gov/newsroom/alerts/new-stem-resources-available-on-uscis-website.

[51] For example, see, *Getting Skills Right: Assessing and Anticipating Changing Skill Needs*, OECD, 2016, www.oecd.org/publications/getting-skills-right-assessing-and-anticipating-changing-skill-needs-9789264252073-en.htm.

mechatronics, machining, and other hands-on skills needed to complement coursework in advanced manufacturing, including semiconductor fabrication and design tools. Similar shortcomings exist in colleges and universities where many computer science and engineering departments no longer offer courses providing practical experience in circuit design, fabrication, and testing. Relevant, experiential training is crucial for high-skilled jobs in microelectronics—coursework is not enough. Moreover, in the most highly specialized areas, exposure to and mentorship by established industry professionals as instructors or through internships and apprenticeships is necessary to acquire the most up-to-date skills.

Strategies to provide experiential training include:

- A public-private microelectronics training system incorporating apprenticeships, internships, co-ops, and other on-the-job training opportunities responsive to the pace of microelectronics technology development and innovation, developed through collaboration among agencies, and with academic, industry, professional societies, State and local educational stakeholders, and international allies.
- Investments to incentivize on-the-job training models through internship and apprenticeship programs at both public and private-sector research laboratories, development centers, and manufacturing facilities.
- Promoting and supporting cross-disciplinary and cross-sector exposure through development of “co-design” studios.
- Developing and facilitating regional access to both fabrication (industry) and “fab-less” resources. As new domestic fabrication, test, and packaging facilities come online, clear mechanisms need to be established for student and faculty access complemented by financial support for their participation.
- Encouraging appropriately vetted international student exchanges to further broaden access to fabrication facilities and secure cooperation with international allies.

Strategic Objective 2.3. Support a future-focused workforce.

Many American microelectronics industry workers undergo some form of retraining during their careers, which may take place through educational institutions, employers’ R&D laboratories, and/or on the job. As the pace of innovation in the industry accelerates, it is increasingly imperative that workers have life-long learning opportunities to keep pace with advances in technology. Learning and up-skilling opportunities should be available to all Americans. The needed expertise, skills, and workforce composition vary along the supply chain. Moreover, as the supply chain evolves over time, different academic backgrounds will become more or less relevant to the health of U.S. firms. Providing continuous learning opportunities will therefore be essential to preventing skill shortages that hinder industrial innovation and skill mismatches that reduce productivity—problems the United States is already facing in high-technology industry sectors.

Access to good information on the current and anticipated skills needed within the industry will be an important element to designing policies to meet those needs. Such information will be required to design apprenticeships, retraining courses, and on-the-job training programs as well as for future curriculum development, technical and vocational education, and career guidance for learners. Some of these skills may be new to the industry as it evolves to meet growing markets and new technologies such as clean energy and digital manufacturing. Similarly, advances in technology may create new opportunities in the semiconductor industry to workers from other high-skill sectors.

Developing and sustaining a needs-based, future-focused microelectronics workforce will require strong coordination in the collection and use of skill-need inventories among educators, policy makers, the labor market, and industry. Connecting, scaling up, and amplifying successful programs will be critical to meet the future workforce needs of the semiconductor industry and ensure U.S. leadership in microelectronics.

Programs that can serve as examples and/or resources for future efforts include:

- The NSF-supported *Preparing Technicians for the Future of Work,*[52] that has demonstrated success in promoting regional collaboration between community colleges and industry and their workforce development professionals to determine the technical demands of the future.
- An NSF-supported project to develop the talent pipeline for the semiconductor industry that connects industry, talent, and education to create a competency-based Industry Approved Apprenticeship Program.[53]
- The MEP National Network™ that provides resources to help small and medium-sized manufacturers grow and thrive.[54].
- TechHire, launched in 2015 and now supported under Opportunity@Work,[55,56] offer models for expanding the range of talent who can access technology industry training and jobs.[57]

[52] http://www.preparingtechnicians.org
[53] www.semi-works.com.
[54] www.nist.gov/mep.
[55] https://obamawhitehouse.archives.gov/issues/technology/techhire
[56] https://opportunityatwork.org/.
[57] techhire.org.

Goal 3. Facilitate the Rapid Transition of R&D to U.S. Industry

The U.S. microelectronics industry accounts for nearly half of global sales in the sector and is highly competitive—and in many cases leads—in R&D and manufacturing technologies.[58] However, the United States no longer has the broad leadership in manufacturing across business segments that it had in past decades. The diminished U.S.-based manufacturing capacity threatens the important linkage between manufacturing and R&D productivity that is an essential component of innovation in this industry. To maintain and enhance global leadership in the sector, the United States must strengthen and accelerate the transition of R&D to both U.S. and allied industry and public sector end users.

Four decades ago, the U.S. semiconductor industry also faced significant international economic competition, leading the U.S. Government to support SEMATECH as a public-private partnership to reestablish U.S. leadership in semiconductor manufacturing.[59] With time, the consortium became independent from Federal funding and expanded to include international partners. Now, the stakes are even higher. Not only has international competition intensified, but technical challenges to increasing performance and scaling, along with the introduction of novel architectures and computing paradigms discussed above, requires an effort with a much broader focus supported by new modes of collaboration and partnership that draw on the lessons learned from SEMATECH and other preceding partnerships.

There is strong agreement among public and private-sector stakeholders that maintaining leadership in this industry will require the United States to innovate *at a faster pace* than competitors.[60] Accelerating the rate at which R&D is translated into products and services is essential to deriving broad benefits for the public, supporting the U.S. economy, and sustaining national security. A vibrant culture of innovation, as addressed in Goal 1, is a critical foundation that must be complemented by resources and policies to accelerate the transition of those innovations. Sustained leadership requires the creation and support of a virtuous cycle, where R&D drives innovative market-ready technology development, and in turn those technologies drive new insights and funding for R&D. This combination of excellence in R&D coupled with *rapidly* transitioning R&D into products and services will be an essential and distinctive competitive advantage for the United States and its allies.

New technology approaches often take 10–15 years from the time research is published to when the innovation reaches wide-scale commercial manufacturing. Innovations that rely on complex scientific breakthroughs can take substantially longer, as seen, for example, with extreme ultraviolet lithography tools, which took more than 40 years to be incorporated into high-volume manufacturing. The long-

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[58] For example, see *2020 State of the U.S. Semiconductor Industry,* Semiconductor Industry Association, www.semiconductors.org/wp-content/uploads/2020/06/2020-SIA-State-of-the-Industry-Report.pdf.

[59] *SEMATECH: Progress and Prospects*, Advisory Council on Federal Participation in SEMATECH, 1989, www.esd.whs.mil/Portals/54/Documents/FOID/Reading%20Room/Science_and_Technology/10-F-0709_Report_of_the_Advisory_Council_on_Federal_Participation_in_SEMATECH_1989.pdf.

[60] For example, see *Report on Ensuring Long-Term U.S. Leadership in Semiconductors,* Presidents Council of Advisors on Science and Technology, 2017, obamawhitehouse.archives.gov/sites/default/files/microsites/ostp/PCAST/pcast_ensuring_long-term_us_leadership_in_semiconductors.pdf; *Winning the Future. A Blueprint for Sustained U.S. Leadership in Semiconductor Technology*, Semiconductor Industry Association, 2019, www.semiconductors.org/wp-content/uploads/2019/04/SIA_Winning-the-Future_Refresh_FINAL1.pdf; and *Final Report*, National Security Commission on Artificial Intelligence, 2021, www.nscai.gov/wp-content/uploads/2021/03/Full-Report-Digital-1.pdf.

time horizons needed to transition R&D into commercial practice present a barrier that Federal support and enhanced coordination across stakeholders may help surmount by accelerating innovation across the research, development, demonstration, and deployment pipeline.

Innovation in microelectronics occurs within a wide range of organizations including academic institutions, industry, government facilities, Federally Funded Research and Development Centers, and nonprofit laboratories. Large and small companies across the microelectronics supply chain, from materials suppliers to manufacturers—including start-ups, fabless design companies, foundries, integrated device manufacturers, and product, platform, and service providers—are critical to the innovation ecosystem. These entities provide multiple paths for innovation to transition into manufacturing. This strategy aims to facilitate the transition of technology across and among all these pathways by strengthening the entire microelectronics R&D innovation ecosystem in the United States. These efforts will increase collaboration across technology development pathways and build out and bridge the microelectronics infrastructure from research to manufacturing.

Strategic Objective 3.1. Increase collaboration across technology development pathways.

Deeper collaboration and communication are needed within and between the R&D and end-user communities in both industry and government along the entire technology development pathway. Better integration between these communities will help to ensure that R&D is focused on the topics most likely to result in broad and transformational benefits while also enhancing the likelihood that breakthroughs from early-stage R&D attract the follow-on domestic and allied investments needed for transition.

Key Strategy 3.1.1: Facilitate academic, government, and industrial exchange to promote collaboration and broaden understanding of needs and opportunities.

Mechanisms are required to increase communication among academic, government, and industrial R&D communities. Such communication is essential for connecting R&D performers with end users in government and industry, enhancing researchers' knowledge of system-level design and performance constraints. Enhanced communication can inform research directions to ensure that advancements can be implemented and increase the likelihood that innovative concepts are transitioned to manufacturing.

In addition to student internships, opportunities for faculty to spend time in industrial R&D or manufacturing settings, or in federal research facilities, can provide valuable experience and insight. Likewise, embedding industry researchers in academic centers can promote information exchange and provide context to the university research community.

Federal agencies regularly collaborate directly with companies from across the microelectronics sector on research areas of mutual interest, and industry may engage directly with individual academic research groups for specific programs. Public-private partnerships (PPPs), where appropriate, however, can bring multiple parties together, and the establishment and sustained support of these efforts can be an effective approach to facilitate collaboration focused on specific technical challenges addressed by strategically assembled teams. For example, some Federal agencies like NSF, have partnered with the Semiconductor Research Corporation (SRC) as an approach to couple fundamental academic research more tightly to longer-term industry technology and workforce needs. The success of this approach is epitomized by the Joint University Microelectronics Program (JUMP) and its predecessors.

While industry often has bilateral agreements with specific academic investigators, federally funded programs such as JUMP facilitate broader cross-industry information exchange and consensus building. With a broader community perspective, these collaboration structures more quickly identify the highest priority fundamental research to fund. These structures also provide rapid feedback from the industry partners to the academic researchers, with government participants helping to ensure a broad impact and public-sector return on investment.

Research partnerships also should include the negotiation of invention rights to achieve mutual benefit for all partners. In evaluating formal research relationships, the review process should assess and mitigate possible risks to the security and integrity of the research enterprise. Such reviews can minimize inappropriate technology transfers and ensure that legitimate R&D collaborations are not converted into covert technology transfers.

The Manufacturing USA Institutes represent another effective model for fostering exchange between industry needs and academic capabilities across multiple manufacturing-based industries. Presently, five institutes support elements of the microelectronics manufacturing base, including the adjacent sectors of additive manufacturing and 3D printing, advanced robotics for manufacturing, and digital tools for manufacturing. Additional engagement with these and other sectors that rely on microelectronics innovation, such as industrial automation and robotics, communications, high-performance and next-generation computing, and artificial intelligence, would help inform new areas for collaboration. Under the CHIPS Acts, Congress authorized and appropriated resources for the establishment of up to three new Manufacturing USA Institutes focused on semiconductor manufacturing. Increased support for new and existing models can extend to new and emerging technologies and engage new industry partners, both large and small, to accelerate the transition of new technologies to manufacturing.

Incentivizing the unique capabilities at existing regional innovation hubs such as “Silicon Valley” in California, “Silicon Gulch” in Texas, and the “Research Triangle” area of North Carolina is an additional strategy to accelerate the identification and commercialization of market-ready R&D projects within these ecosystems. Such hubs can bring together multiple partners and facilitate technology transfer along the lab-to-market pathway by coordination across the supply chain. Partnership-based regional hubs have the potential to reduce the time and cost for development and transition by combining the management capacity of large businesses with the niche expertise residing in smaller businesses, government, and academic research laboratories. Regional hubs have been shown to be most effective when enhancing existing clusters rather than attempting to create such ecosystems without an existing base of capital and talent.[61]

While each of these approaches facilitates knowledge and talent flow within each specific effort, communication across the full microelectronics technology development continuum must be facilitated to support and strengthen the entire ecosystem. Community-building activities under Goal 1 will assist in this task, along with activities associated with the facilities discussed below.

[61] Rethinking Cluster Initiatives, 2018, https://www.brookings.edu/wp-content/uploads/2018/07/201807_Brookings-Metro_Rethinking-Clusters-Initiatives_Full-report-final.pdf

Key Strategy 3.1.2: Support entrepreneurship, start-ups, and early-stage businesses through targeted programs and investments.

The history of Silicon Valley is a testimony to the enormous role played by start-ups in driving innovation within the microelectronics sector. However, trends such as the high capital costs to design and fabricate leading-edge circuits and the consolidation of the manufacturing sector have created a particularly large mismatch between the needs of start-ups and how innovation occurs in large multinational corporations. In view of these challenges, targeted Federal investments are needed to catalyze the creation and promote the success of early-stage companies striving to bring new technologies to market.

Federally funded programs can provide entrepreneurs with business-development training and access to R&D infrastructure, and can help initiate private-sector partnerships and capital investments. Multiple Federal programs have been established to support entrepreneurship that could be scaled and/or replicated to provide opportunities specific to this sector, including the following examples:

- The Innovation Corps (I-Corps) program at NSF provides training to academics to facilitate the formation of start-ups by advancing their understanding of business planning and entrepreneurial skills. DOE's Energy I-Corps does the same for entrepreneurs based at DOE National Laboratories.
- The NSF Convergence Accelerator provides researchers and innovators with the knowledge and opportunity to accelerate solutions into real-world applications by supporting interdisciplinary teams comprised of diverse expertise, disciplines, sectors, and communities of practice working together to stimulate innovation and discovery.
- DOE's Advanced Manufacturing Office has established embedded entrepreneur programs at four DOE National Laboratories to help innovative start-ups develop new manufacturing technologies and bring them to market more quickly through access to the lab's expertise and scientific infrastructure.[62]
- The NIST Technology Maturation Accelerator Program provides a platform for NIST researchers to pitch cutting-edge technologies to venture capitalists and business experts, with the winners to receive funding to accelerate their projects toward the market.
- NASA launched an Entrepreneurs Challenge to identify innovative ideas and new participants that will lead to new instruments and technologies with the potential to advance the agency's science mission goals.
- DARPA created the Embedded Entrepreneurship Initiative to accelerate the commercialization of sponsored research. The initiative funds development of a market strategy, and teams with In-Q-Tel's IQT Emerge to provide mentorship and investor connections. DARPA has also leveraged the Cyclotron Road site from DOE's Lab-embedded Entrepreneurship Program to sponsor fellowships specifically for microelectronics start-ups.

Agency Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs offer another opportunity to support small businesses, both through non-dilutive capital investments and through a wide range of support services to promote the success of the supported companies. There are examples where agencies have coordinated their SBIR/STTR solicitations to

[62] DOE AMO's Laboratory Embedded Entrepreneurship Program (LEEP), https://www.energy.gov/eere/amo/lab-embedded-entrepreneurship-program.

support specific technologies of common interest. Coordinating SBIR/STTR topics across agencies can signal commitment and interest in U.S. innovation and emerging technologies, especially for start-ups and small businesses in fields related to the semiconductor industry. As an example, USDA-NIFA's SBIR/STTR program has funded a project that applies microelectronics technologies to agriculture, including a micro-sensor suite that provides the grower with a direct physical measurement of plant water stress for the purpose of irrigation scheduling. Joint agency topics can be used to establish a wide community-of-practice that intentionally incorporates innovative small businesses and expands connections with accelerators at universities, including at HBCUs and other MSIs.

The United States Air Force's commercial 'investment' group, AFVentures, is an example of an approach for leveraging an SBIR/STTR program to accelerate technology transition by providing additional funds to match private investments in companies in the portfolio.[63] This program increased the percentage of companies with awards that have received some form of venture capital to 29%, as compared to only 10% across all DOD awardees prior to 2015.[64] The AFVentures portfolio presently includes electronics companies as only a small portion of the total awards.

There are a few Federal Government programs that use venture funds for equity financing to directly support early-stage companies and partner with the private-sector venture community. For example, In-Q-Tel supports technologies for the intelligence community and the recently launched BARDA Ventures supports medical countermeasures for public health. Coupling venture capital funds to research infrastructure through PPPs that incorporate technology transfer objectives has shown proven returns in the microelectronics sector in other countries.[65] The venture funds can provide a more direct pathway to support commercialization of the innovations created at the PPP facility.

Loans and loan guarantees are another mechanism that can assist early stage companies. The SBA reduces risk and enables easier access to capital by working with lenders to provide loans to small businesses. The DOE Loan Programs Office administers three distinct loan programs that provide first-of-a-kind projects with access to debt capital that is not available from private lenders, with flexible, custom financing.[66]

In addition to directly supporting and fostering collaborations, start-ups and early-stage businesses must have the opportunity to contribute to setting international technical standards. By participating in international standards-setting activities organized through professional societies or industry associations, the United States can shape global technology development and support access to future international markets. Standards-setting activities can take several years of deliberation before settling on a consensus. New mechanisms to support participation in the development of standards activities would enable much needed participation by small businesses pursuing emerging technologies that have not yet established a commercial market.

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63 https://afwerx.com/afventures-overview/

64 AFVentures FY18–FY20 Impact Report, 2021, https://afwerx.com/wp-content/uploads/2021/10/AFVentures-2020-Annual-Report.pdf

65 For a comparison of models, see: Peña, Vanessa, Marko M.G. Slusarczuk, Jay Mandelbaum, Margaret A. Tucker, Abby R. Goldman, Emily R. Grumbling, and Emma Thrift, *Lessons Learned from Public-Private Partnerships (PPPs) and Options to Establish a New Microelectronics PPP*, Institute for Defense Analysis: Washington D.C., July 2021.

66 https://www.energy.gov/lpo/loan-programs-office.

Key Strategy 3.1.3: Expand the range of industry participants in Federally sponsored R&D.

Efforts to raise awareness of collaborative R&D opportunities and to engage with industry throughout the microelectronics ecosystem need to be amplified to ensure that America benefits from its full innovation capacity. Many potential industry partners with capabilities to support U.S. leadership in microelectronics, including increasingly those from allied countries, do not regularly do business with Federal agencies and may not have financial systems optimized or structured to readily meet the accounting requirements for Federal contracts. Departments and agencies should leverage the full scope of their respective authorities to enable active engagement from the wide range of companies across the entire technology development pathway.

Focused use of Other Transaction Authority (OTA) can be an effective approach to broaden the range of industry partners interested in participating in Federal advanced development programs.[67] DARPA's Electronics Resurgence Initiative (ERI) was established to enhance government-industry partnership in the sector by sponsoring dual-use research. OTAs have been used to broaden participation in ERI's research programs. Through 2021, ERI funded more than 30 agreements for research at non-traditional performers that would typically have not submitted a proposal, including large companies and start-ups. This concerted effort to engage a wider range of companies created direct pathways to transition microelectronics R&D into dual-use commercial products.

Key Strategy 3.1.4: Establish a Microelectronics Industrial Advisory Committee.

Strengthening and revitalizing U.S. leadership in microelectronics will require close engagement, advice, and oversight from a broad cohort of industry and academic stakeholders. As called for in Section 9906(b) of the CHIPS for America Act of 2021, the Secretary of Commerce is establishing an Industrial Advisory Committee to assess and provide guidance to the U.S. Government on the science and technology needs of the Nation's domestic microelectronics industry; analyze the extent to which this National Strategy on Microelectronics Research is helping maintain U.S. leadership in microelectronics manufacturing; assess the research and development programs and activities authorized under the CHIPS for America Act of 2021; and identify opportunities for new public-private partnerships to advance microelectronics research, development, and domestic manufacturing. This committee, which will provide regular reports to the Secretary of Commerce, will also be valuable in proactively identifying emerging R&D, manufacturing technology, and workforce needs in response to future strategic shifts in commercial markets or geopolitics.

[67] See, generally, discussions of OTA at: *Prototyping Using Other Transactions: Case Studies for the Acquisition Community*, RAND, 2020, www.rand.org/pubs/research_reports/RR4417.html; *Department of Defense Other Transactions Authority Trends: A New R&D Funding Paradigm?*, Center for Strategic and International Studies, 2020, www.csis.org/analysis/department-defense-other-transaction-authority-trends-new-rd-funding-paradigm; and *Acquisition in the Digital Age: Other Transaction Authority (OTA)*, MITRE, 2021, aida.mitre.org/ota; Buying What Works: Case Studies in Innovative Contracting, OSTP, 2014, https://obamawhitehouse.archives.gov/blog/2014/08/21/buying-what-works-case-studies-innovative-contracting

Strategic Objective 3.2. Build out and bridge microelectronics infrastructure from research to manufacturing.

As emphasized throughout this strategy, microelectronics R&D is extremely infrastructure-intensive, and access to the appropriate facilities and associated expertise is necessary at every development stage—from discovery through manufacturing. Every development stage must be connected to assure that new innovations can rapidly progress along the technology development pathway. Currently, the United States does not have centralized, open-access facilities for microelectronics R&D that are equipped with fabrication tools, testing, and expertise relevant to a manufacturing environment for leading edge technologies. Therefore, researchers conducting early-stage R&D have limited opportunities to use manufacturing-relevant tools and facilities. Furthermore, the continued diversification of microelectronics innovations results in a complex set of needs across the various R&D stakeholders. Recognizing this current gap in the ecosystem, Congress authorized and appropriated resources for several programs in the CHIPS Acts to help address this is issue (enumerated above in the Introduction).

As further advances in many areas of semiconductor fabrication and microelectronics technology are challenged by the limits of physics and escalating capital costs for manufacturing at these limits, it becomes increasingly important to establish resources that support domestic research maturation and access to advanced prototyping using manufacturing-relevant equipment. The needed resources to enable researchers access to manufacturing relevant R&D facilities include easily accessible facilities in the United States equipped with fabrication tools and testing capabilities to demonstrate the potential of new devices, interconnects, circuits, systems, and fabrication processes in a leading-edge (or near-leading-edge) manufacturing environment. A well-coordinated constellation of facilities with leading-edge equipment and design tools will be essential for advancing leadership in heterogeneous integration — i.e. successfully integrating new technologies with mature design elements at wafer scale, such as combining novel memory devices or interconnect technologies with standard driver circuits or processor nodes.

Key Strategy 3.2.1: Expand access to advanced cyberinfrastructure for modeling and simulation.

Innovation at the limits of physics, manufacturing, and metrology requires that advanced understanding of circuit performance and manufacturing processes be demonstrated in digital simulation before investing in advanced prototyping. Improved modeling and simulation tools that fully leverage high-level synthesis of hardware accelerators and system simulations for circuits and systems are needed, especially those based on novel materials, devices, interconnects, and architectures integrated with CMOS. Furthermore, access to leadership-class computing and other cyberinfrastructure, including at National Laboratories and NSF-funded facilities, along with close coordination among users, system developers, and prototyping facilities, is required. These capabilities need to be closely connected with the physical infrastructure to best support the R&D community and assist with technology transfer.

Key Strategy 3.2.2: Establish the National Semiconductor Technology Center to support advanced research, development, and prototyping.

Access to advanced prototyping resources available through the National Semiconductor Technology Center (NSTC), or a constellation of integrated facilities, as authorized and funded by the CHIPS Acts, will provide critical, domestic capabilities to put research innovations more rapidly onto silicon wafers using leading-edge CMOS processes. Two factors strongly argue for the U.S. Government investments in an accessible set of advanced prototyping resources: the high cost to establish, operate, and maintain facilities capable of fabricating leading-edge electronics; and the compelling need to establish and maintain consistent process standards and control. Providing access to well-maintained and tightly integrated resources will also maximize the opportunities for informal learning and collaboration between students, researchers, and industrial and government end users.

The NSTC will provide advanced prototyping capabilities to address the broad needs of the U.S. research community. Important features of the NSTC will include the capability to perform materials characterization, instrumentation metrology, and testing for advanced process nodes. These capabilities would enable organizations beyond just the established integrated device manufacturers to perform this type of research and increase the range of R&D that larger companies can quickly advance into manufacturing. For researchers to receive feedback from industrial end users, the NSTC must be aligned with and in coordination with the packaging program described in key strategy 3.2.3, provide access to advanced test, assembly, and packaging capabilities for advanced nodes, as well as support advances in automation in manufacturing in order to provide a foundation for increasing the future U.S. share of global manufacturing capacity and competitiveness.

In addition to supporting scale up and prototyping of transformational semiconductor and microelectronics technologies and processes, a core function of the NSTC as authorized and appropriated in the CHIPS Acts is "…to establish an investment fund, in partnership with the private sector, to support startups and collaborations between startups, academia, established companies, and new ventures, with the goal of commercializing innovations that contribute to the domestic semiconductor ecosystem, …". To accomplish this function, the NSTC could look to models such as In-Q-Tel and other similar venture funds and incubators. The NSTC could establish an affiliated 501(c)(3) nonprofit or similar organization with the responsibility of evaluating entrepreneurial semiconductor companies and technologies emerging from early-stage R&D investments from NSF, DOE, and DOD, or companies spun out of projects supported through the NSTC. Based on the ability of the firms to meet a defined set of evaluation criteria, the affiliated 501(c)(3) nonprofit could provide access to capital through loans, grants, or other financial instruments, together with technical assistance and consultation.[68]

Once established, this PPP will serve as a focal point for the entire microelectronics ecosystem and facilitate communication across all stages of R&D through manufacturing.

Key Strategy 3.2.3: Support advanced assembly, packaging, and test.

Innovations in the packaging, assembly, and testing of microelectronic components is key to continued U.S. leadership. As semiconductor fabrication reaches the limits of performance and efficiency improvements attainable by reducing the transistor feature size, industry has turned to new approaches for higher-performance enabled by 3D systems and heterogeneous integration. The current generation of high-performance devices integrate multiple technologies that include not just different silicon-based processes but also compound semiconductors and other specialized technologies. Both approaches place much greater demands on the ability to interconnect devices and

[68] CHIPS for America Act of 2021 §9906(c).

subsystems—a key aspect of advanced packaging. Improvements in interconnect technology and standards for 3D and heterogeneous integration could also foster the development of a new supply chain structure for microelectronics where domestic capabilities would enhance U.S. security and competitiveness.

Advanced test, assembly, and packaging capabilities are also needed for validation of advanced prototypes that emerge from the R&D process. As authorized and appropriated by the CHIPS Acts, DOC will lead new efforts to establish an advanced packaging manufacturing program to strengthen domestic capabilities. Capabilities supported will include metrology and lithography for manufacturing, including material characterization, instrumentation, testing, and standards. The program will also provide support for advanced packaging efforts aligned with the NSTC outlined in key strategy 3.2.2. As trends in leading-edge electronics are increasingly moving toward advanced heterogeneous integration, the overlap between advanced packaging and prototyping is expected to increase substantially; as is the case for other aspects of microelectronics innovation, the development and deployment of assembly, packaging, and test capabilities needs to be coordinated across the ecosystem, with open communication between the manufacturing and R&D communities.