PCAST Report on Revitalizing the U.S. Semiconductor Ecosystem

Wednesday September 7, 2022

PCAST Working Group on Semiconductors

Co-Leads: Bill Dally* (NVIDIA) & Lisa Su* (Advanced Micro Devices [AMD])

Members: Ahmad Bahai (Texas Instruments)

Anantha Chandrakasan (MIT)

Scott DeBoer (Micron)

Dario Gil (IBM)

Andrea Goldsmith* (Princeton University)

Ann Kelleher (Intel)

Tsu-Jae King Liu (University of California, Berkeley)

Priyanka Raina (Stanford University)

Pete Rodriguez (Silicon Catalyst)

* Denotes PCAST member

Report Focus and Findings

Key Question

How can the United States make the most of the CHIPS and Science Act to ***revitalize the semiconductor ecosystem in the face of growing global competition***?

Key Findings

- A healthy, U.S.-based semiconductor ecosystem is ***vital to our economic prosperity and national security***
- The ***U.S. leads the world in semiconductor-related revenue, but our leadership has been declining*** in recent years, while semiconductor capabilities have been increasing in other countries, particularly in Asia
- ***Startups have been a key driver*** of the semiconductor ecosystem's success since its inception
- Bold actions are required now to ***invest in, develop, and implement a comprehensive strategy*** that rebuilds the domestic semiconductor ecosystem

Report Recommendations

Report Scope

- Implementation of the $11B specifically appropriated for research and development through the CHIPS and Science Act

Recommendations

- Build a broad coalition – Bring the entire U.S. semiconductor ecosystem together in public-private partnership
- Semiconductor workforce development – Form a national microelectronics training network
- Foster innovation – Reduce the barriers of entry to startups
- Set a national semiconductor research agenda with fundamental research and nationwide grand challenges

Recommendation 1

The Secretary of Commerce should establish NSTC* as an independent legal entity in public-private partnership by the end of 2023. The Secretary of Commerce should select a Board of Directors and that Board should oversee both the NSTC* and the NAPMP** to ensure synergy and alignment in the investments. The Board members should include broad representation from government, industry, and academia.

*NSTC = National Semiconductor Technology Center

**NAPMP = National Advanced Packaging Manufacturing Program

Recommendation 2

The Secretary of Commerce should ensure that the NSTC founding charter includes establishing prototyping capabilities in a geographically distributed model encompassing up to six coalitions of excellence (COEs) aligned around major technical thrusts such as advanced logic; advanced memory; analog and mixed-signal; life science applications; design and methodologies; and packaging. The packaging COE should encompass the budget and the objectives of the NAPMP initiatives.

Recommendation 3

The Secretary of Commerce in coordination with the Director of the National Science Foundation should support the establishment of a national microelectronics education and training network by the end of 2023 and allocate funding on the order of $1B over the next 5 years to upgrade educational laboratory facilities, support curriculum development, and facilitate hiring of faculty into this field.

Recommendation 4

The Secretary of Commerce should ensure that NSTC-funded research (discussed in Recommendation 8) supports on the order of 2,500 scholarships and research assistantships per year across the educational spectrum.

Recommendation 5

The Department of Homeland Security should implement existing statutory and regulatory authorities to provide premium processing to newly filed Immigrant Petitions for employment-based second preference advanced degree immigrants seeking a National Interest Waiver to work in microelectronics endeavors.

Recommendation 6

The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an investment fund on the order of $500M to provide financial support and in-kind access to prototyping and tools for semiconductor startups.

Recommendation 7

The Secretary of Commerce should ensure that the NSTC creates or funds the creation of a “chiplet” platform* with a complete software stack by the end of 2025 so that startups and academic institutions can integrate their custom chiplet(s) with the NSTC-supported chiplet platform to demonstrate new innovations with dramatically reduced investment and time.

*A chiplet platform is an integrated circuit that is composed of multiple smaller chips where the common, non-innovative parts of a product have been specifically designed so that customizable components (“chiplets”) can be added to address particular applications, performance, or functionality.

Recommendation 8

The Secretary of Commerce should ensure that the NSTC founding charter allocates a significant portion of the annual funding, on the order of 30-50 percent, to directly fund a national research agenda. This research agenda should be broad in nature and address the following areas: materials, process, and manufacturing technologies; packaging and interconnect technologies; energy-efficient computing and domain-specific accelerators; design automation tools and methods; semiconductor and system security; and semiconductors and life sciences.

Recommendation 9

The NSTC should identify a set of nationwide grand challenges that are enabled through collaboration across the NSTC industrial membership and NSTC-funded research. These grand challenges should span three complementary areas that would benefit from large-scale nationwide collaboration: advanced computing into the zettascale* era; significantly reducing design complexity; and proliferating semiconductors in life sciences applications.

* 1 zettaflop = 10^3 exaflops = 10^{21} floating point operations per second

Recommendation 10

To improve visibility into federal semiconductor investment efforts, measure the progress across the industry at the federal level, and maximize the leverage of such investments, we recommend the following:

(A) Starting in 2023, and annually thereafter, the Networking and Information Technology Research and Development (NITRD) program — a subcommittee of the National Science and Technology Council — should collate and publish annual investment figures for semiconductors across all federal agencies.

(B) The Department of Commerce-led NSTC should encourage all agencies with semiconductor R&D investments to leverage and utilize the NSTC facilities and capabilities. We recommend the NSTC expand and co-fund programs with other agencies and in public-private partnership where the research agendas are synergistic including, for example, DARPA's Electronics Resurgence Initiative (ERI), Research on the Future of Semiconductors sponsored by the Computer and Information Science and Engineering (CISE) Directorate at NSF, and the broad multi-sector collaborations enabled by the Semiconductor Research Corporation (SRC).

(C) The Secretary of Commerce should develop and regularly evaluate performance measures to assess progress, effectiveness, outcomes, and impact of the CHIPS and Science Act initiatives and report them annually to the President.