Public Meeting of the

President's Council of Advisors on Science and Technology (PCAST)

May 12, 2022

Meeting Minutes

Meeting Participants

PCAST Members

1. Frances Arnold, Co-Chair
2. Francis Collins, Co-Chair
3. Maria T. Zuber, Co-Chair
4. Dan E. Arvizu
5. Dennis Assanis
6. John Banovetz
7. Ash Carter
8. Frances Colón
9. Lisa A. Cooper
10. John O. Dabiri
11. William Dally
12. Sue Desmond-Hellmann
13. Inez Fung
14. Andrea Goldsmith
15. Laura H. Greene
16. Paula Hammond
17. Eric Horvitz
18. Joe Kiani
19. Jon Levin
20. Steve Pacala
21. Saul Perlmutter
22. William Press
23. Penny Pritzker
24. Jennifer Richeson
25. Vicki Sato
26. Lisa Su
27. Kathryn Sullivan
28. Terence Tao
29. Phil Venables
30. Catherine Woteki

PCAST Staff

1. Anne-Marie Mazza, Executive Director
2. Reba Bandyopadhyay, Deputy Executive Director
3. Sarah Domnitz, Deputy Executive Director and PCAST Designated Federal Officer
4. Kevin Johnstun, Research Analyst

Invited Speakers (in order of presentation)

1. Pat Gelsinger, Chief Executive Officer, Intel
2. Priyanka Raina, Assistant Professor of Electrical Engineering, Stanford University
3. Rodrigo Liang, Chief Executive Officer and Co-founder, SambaNova
4. Aart DeGeus, Co-founder, Synopsys

5. John Neuffer, President and Chief Executive Officer, Semiconductor Industry Association

START DATE AND TIME: Thursday, May 12, 2022, 2:00 PM Eastern Time

LOCATION: Virtual Meeting via Zoom.gov

WELCOME

PCAST Co-chairs: Frances Arnold, Francis Collins, Maria Zuber

The PCAST co-chairs – Frances Arnold, California Institute of Technology; Francis Collins, Acting Science Advisor to the President; and Maria Zuber, Massachusetts Institute of Technology -- called the meeting to order. After Arnold introduced a new member of PCAST, Dennis Assanis, President of the University of Delaware, Zuber provided introductory remarks. She noted that other countries are investing significant resources to build semiconductor manufacturing capability and develop a skilled workforce, steps that seriously challenge the preeminent position that the United States has held in semiconductors, and microelectronics more generally. Already, Taiwan and South Korea have established enviable competitive positions in the production of high-end chips, and U.S. technology firms depend on Taiwan to manufacture a large percentage of their chips. Zuber noted that PCAST has a strong interest in U.S. leadership in semiconductors and looks forward to an engaging session.

SESSION: CHALLENGES AND OPPORTUNITIES FOR U.S. LEADERSHIP IN SEMICONDUCTORS

Pat Gelsinger, Intel

Pat Gelsinger began his remarks by noting that as a result of the digital transformation occurring today, every aspect of society is increasingly running on semiconductors. To keep pace with this rapid transformation, the United States needs to continue building leading-edge semiconductor capabilities, and the federal government needs to invest significantly more in developing those capabilities to ensure the U.S. semiconductor industry's health and leadership in this area. In that regard, the National Semiconductor Technology Center (NSTC), conceived as part of the Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act that is now before Congress, will play a critical role in helping the United States maintain its leadership in semiconductor research and development and in the development of the future semiconductor workforce.

Gelsinger said that Intel spends about 20 percent of its revenue, or just over $15 billion in 2021, on research and development activities, making it one of the most intensive research and development companies in the world. He added that the company manufactures the majority of its products in the United States. Over the past year, Intel has laid out what he called a bold investment strategy to help rebuild U.S. leadership in manufacturing computer chips using the world's most advanced technologies. That said, the company believes that public-private partnerships are essential for rebuilding semiconductor manufacturing capacity in the United States. The federal government, which played a seminal role in the birth of the semiconductor industry, should now play a critical role in enabling the

future success of the U.S. semiconductor industry, said Gelsinger. Semiconductor technology is at an inflection point, he added, and without action, the U.S. industry will see a continued decline in its ability to compete globally. Action on the part of the federal government, however, can lead to a meaningful increase in U.S. semiconductor manufacturing.

The demand for low-latency, high-performance, higher-density chips is almost inexhaustible, said Gelsinger, driven by the increasing use of simulation, be it in developing new medicines, creating metaverses, establishing digital twins for product development, or in other emerging applications. Intel, he said, just launched its zettascale computing initiative to enable 10^{21} operations per second within the next five years and deliver petascale, or 10^{15} operations per second, computing speed to every human on the planet. He predicted that by the second half of this decade, manufacturers will use advanced lithographic modes such as extreme ultraviolet lithography on over 40 percent of the wafers it processes. Few companies, however, will have both the research and development capacity and the capital capacity to participate in these advanced manufacturing modes, which is why federal level action is needed. Gelsinger remarked that if geopolitics was defined over the past five decades by where oil reserves exist, the next decades will be defined by where semiconductor fabrication plants (fabs) are located.

Gelsinger said NSTC should comprise a set of nationwide hubs placed with U.S. companies and other facilities to leverage existing infrastructures, minimize costs to build new infrastructure, and maximize the bridge between the public and private sectors. Intel has proposed serving as one of the hubs, at least in the areas of advanced lithography and advanced packaging technology. Gelsinger said that in his view, there are significant areas in which revolutionary breakthroughs will occur. To enable these advances, NSTC should fund both early-stage, pre-competitive research and development activities as well as late-stage work to ensure that prototyping and other efforts are integrated into the nation's supply chains. Such efforts, he said, should focus on delivering manufacturing at scale in the United States.

Gelsinger recommended that NSTC develop a multi-year roadmap of projects and long-term objectives. A technical advisory committee that includes experts from industry and academia should constantly vet the roadmap and objectives to ensure that they meet the future needs of the U.S. semiconductor industry. He also said that the federal government should allow NSTC to be an independent entity in order to mitigate conflicts of interest, and that the federal government and the private sector should both fund NSTC to enable its long-term viability.

Turning to the subject of workforce development, Gelsinger noted that establishing technological leadership means having the right people and leadership in areas such as research, design, manufacturing, and packaging, and a reliable workforce with training in science, technology, engineering, arts, and mathematics. Demand for such a workforce is forecasted to grow at 10 percent per year this decade, but U.S. students are choosing to focus on computer science rather than on semiconductor manufacturing. To bring vibrancy back to this area, he recommended removing institutional barriers; increasing access to state-of-the-art science, technology, engineering, and mathematics education; and reaching into diverse communities to draw students to the field. In that regard, the CHIPS Act should include funds to increase grants and research fellowships at the collegiate level and develop educational programs that reach into high schools.

Intel, said Gelsinger, is committed to doing its part in this effort, and toward that end, it will invest $100 million over the decade to establish semiconductor manufacturing in Ohio. Some of those funds will go

to a partnership with the National Science Foundation (NSF) and Midwest universities and research institutions to expand workforce development programs. In fact, Intel has developed a number of successful workforce development programs that community colleges and high schools can replicate.

Gelsinger concluded his remarks by noting that it has been about 50 years since semiconductors began shipping commercially. Today, he said, they are the foundation for virtually all forms of technology innovation, and yet he said he thinks that the world is now entering into a golden age for semiconductors. As such, he believes there is a narrow window to take decisive actions to capitalize on this inflection point. Intel has pledged to take such actions, making significant investments that for the first time in four decades will be greater than the company's free cash flow. As a final comment, he said that the depth and breadth of the nation's research efforts on silicon platforms, software, new materials, at-scale manufacturing, and advanced two-dimensional and three-dimensional packaging, along with the relentless pursuit of Moore's Law, provide an extraordinary opportunity for the United States to continue to fuel the global digital renaissance and strengthen the U.S. economy and national defense.

Priyanka Raina, Stanford University

The biggest strength of the United States is its ability to innovate, said Priyanka Raina, but innovation in the semiconductor industry is limited today by three key challenges. The first, she said, is a slowdown of Moore's Law, which means that transistor scaling alone will not on its own lead to cost reductions and improvements in performance and efficiency. The second challenge is the enormous complexity of designing end-to-end hardware/software systems, which makes it difficult for small teams to innovate. In part, that is why student interest in semiconductor design has been declining for the past several years, leading to the current workforce shortage, which is the third challenge.

Raina said these challenges also present a tremendous opportunity for a dramatic reinvention of the system design process. This reinvention will be similar to the one that occurred in the 1980s, when chip design moved from a few large companies with in-house fabs to many small fab-less companies. Electronic design automation (EDA) tools developed then greatly simplified chip design, and in the process made it accessible to a much larger set of people and allowed small companies to innovate.

The question now, said Raina, is how to achieve a similar reinvention today. To start, several areas of research will require investment, such as the design of domain-specific hardware accelerators. These are specialized chips designed for a specific application domain and therefore can achieve higher performance and efficiency than is possible with a general-purpose central processing unit (CPU). These accelerator chips, she explained, are and will continue to be key drivers of large-scale deployment of emerging applications such as machine learning, image processing, video coding, cryptography, and others. Designing these accelerators incurs substantial design, verification, and software engineering costs. In fact, the cost of designing the software stack that allows applications to run on these accelerator chips is much larger than the cost of designing the chip. In total, the cost of designing an accelerator chip is close to $500 million, making it imperative to conduct the research needed to develop tools and methodologies to reduce the design, verification, and software engineering costs.

Raina said that critical areas of research in semiconductor design include developing methodologies that raise the level of abstraction for design and verification of hardware/software systems. Two other critical

areas for research are automated co-design of programmable accelerators and compilers for fast-changing application domains and developing tools for automated, large-scale design space exploration and optimization. Stanford University, for example, has created a system that generates both the hardware accelerator and the software compiler from a single, formal specification of the hardware. Doing so greatly reduces the cost of manually updating the compiler for every hardware change.

Raina also noted that research is needed on how to reduce barriers to entry for semiconductor startups. Startups spend a large fraction of time and investment on non-innovative portions of design. These portions are too complex to build from scratch or to build by putting existing intellectual property (IP) together. She explained that the innovative custom chiplet is only a small fraction of the full system on a chip (SoC) needed to ship a product. Typically, the SoC includes a CPU, a complete memory system, chip-to-chip interfaces, high-speed input/output, a power delivery network, clock generation, and test and debug circuitry. On top of this hardware sits a large software stack for managing interactions between the SoC and the custom chiplet. What is needed to reduce the time to market, she said, is a chiplet ecosystem that provides an existing working platform SoC and software stack to which the designers can attach their innovative chiplets using advanced packaging techniques. In her opinion, such an ecosystem would enable small teams to prototype and demonstrate their ideas with much lower investment, and by doing so, usher in a new wave of innovation and system design, similar to the EDA-enabled revolution of the 1980s.

Addressing the challenge of attracting more students to semiconductor design and manufacturing, Raina noted that students are drawn to fields that capture their interest and imagination, and that requires empowering small groups to innovate and create exciting systems. This is not possible, though, with today's complex approach to chip design, leading to a decline in student interest and a move toward computer science, which allows for faster prototyping and the ability to innovate, create startups, and engage in exciting projects. To counteract this decline, Stanford has introduced new classes into its electrical engineering curriculum that allow students to create and prototype the chips they design in their class projects. These courses have led to a gradual increase in enrollment in both the prototyping class and the feeder class.

Raina then offered a recommendation regarding what U.S. universities need to do to attract more students to electrical engineering rather than computer science. Reinvigorating student interest requires developing more exciting chip design courses that support prototyping of student-designed chips. This will require providing students access to multi-project wafer fabrication runs through a MOSIS-like aggregator, industry-standard EDA tools, and a computing infrastructure on which to run their chip design flows. She noted that providing EDA tools and computing infrastructure is a small problem since most of these capabilities exist, but the fabrication run part is equally important.

The federal government can play a role here, said Raina, by funding universities to develop, maintain, and freely share chip design flows and libraries. This last part is quite important, she noted, because teaching such a class requires a significant effort on the part of faculty and the teaching assistants, and having readily available chip design flows and libraries would allow sharing curricula and flows created at other universities and reduce the burden on instructors. As a final comment, Raina said she would like to see NSTC take on three tasks: support research on tools to dramatically reduce for the cost of design, verification, and deployment of systems with domain-specific accelerators; create a chiplet ecosystem

that provides a platform SoC and software stack to which innovative chiplets can attach using advanced packaging; and reinvigorate student interest in semiconductors by supporting chip design and prototyping classes.

Rodrigo Liang, SambaNova Systems

Rodrigo Liang began his remarks by stating that from a computing perspective, a generational transition is occurring on the scale seen with the World Wide Web in the 1990s and mobile computing in the 2000s. This transition has companies in every industry starting to consider how artificial intelligence (AI) is going to affect their business. The reality, said Liang, is that the implications of AI have yet to be determined given that AI is just starting to take hold in various industries. As with the internet and mobile computing, it will only be in hindsight that massive changes produced by AI will become apparent. For example, in the early days of the Web, companies thought that creating a webpage and showcasing their presence on the internet was enough of an accomplishment, but today the capabilities of the internet are creating entire new economies. AI, predicted Liang, will lead to the creation of new applications, new ways of thinking about problems, and new end-user demographics that will create opportunities and challenges.

Liang said that the advancements in AI spurred venture capital to invest nearly $10 billion in semiconductor startups in 2021, a substantial increase from the minimal interest venture capital showed in the semiconductor space over the past 10 to 15 years. He noted that some analysts predict that AI-related semiconductors could account for as much as 25 percent of all semiconductor demand and will outpace growth of traditional semiconductors. Companies developing application-specific accelerators for AI of the type that Raina discussed are creating excitement around semiconductors, which has led to venture capital firms stepping up their investments.

According to a McKinsey report, AI is expected to add $15 trillion to the global economy over the next century, said Liang. Such a figure might be difficult to comprehend, but it points to the fact that AI offers an unparalleled opportunity to process and use all of the data that has accumulated over the past 10 to 20 years to develop insights and a competitive advantage. Companies are seeing this, he said, and are deploying AI in ways that are not always obvious to gain competitive advantages, and he predicted that companies that are not doing this will quickly find themselves falling behind.

Liang said that semiconductors will play a big role in enabling the United States to use AI to maintain its current competitive advantage on a global scale, and it is imperative to consider how to apply AI across a broad range of applications in the nation's companies and industries. The ability to handle huge amounts of data using semiconductors with specific purpose-designed functionality will be critical to enabling the AI-powered transition that will occur over the next 10 to 15 years, and startups have a role to play here. Startups, he explained, are well suited to working on emerging applications and emergent markets that have not yet reached a scale to make a material financial impact for large companies. The risk of success versus the risk of failure for a typical project will be higher than something that would be attractive to a big company, but that is the perfect role for a startup to play.

Creating a vibrant startup ecosystem, said Liang, requires a funding model that accounts for the fact that developing hardware costs far more than developing software. It also requires market access and figuring out how a product fits a particular market. Addressing market fit is challenging given that the

procurement process, particularly for a large company, can take too long to fit the needs of a startup, which wants to have quick access to a market to see if its product fits. A vibrant startup ecosystem would also benefit from having technology and partners to leverage, as well as standard systems to which a startup can jump in quickly and put an innovative idea in place for further testing. Talent is another imperative for a successful startup ecosystem, and addressing the current talent shortage is a place that needs investment.

Liang discussed the relationship between the time it takes for a startup to reach sustainable profitability and the amount of money that it takes to move through the many stages of product development, from hiring talent and accessing technology, to prototyping and system and software development, to proof-of-concept and volume production. Whereas a large company will have a steady revenue stream to support a development roadmap, startups have to make a significant investment before they make a single dollar. They have to hire talent, build a technology infrastructure, and decide on the chiplet technology and existing IP they will use in their chip design, all prior to even beginning to design a chip. Chip development itself then takes 6 to 18 months to get to the first article and tapeout, the point at which the final design goes to the fab. Then articles come back from the fab in four to eight months, depending on the technology used to create the chip, and that prototype then goes into creating a complete system upon which software development can occur. All together, said Liang, the process can take from two to four years before obtaining a hardware/software product that a potential customer can use to demonstrate proof of concept. In contrast, software startups do not have to access technology, secure time at a fab, or build systems to produce their products. All of this, added Liang, takes cash that startups have to raise through venture capital or other means and that has to last until commercialization occurs. He estimated that it can take $100 million or more for a company to get to a point that it can sustain itself.

A key step in the development process is to get to a point where customers can start conducting proof-of-concept testing. Even then, the chiplet will go through several rounds of testing and making alternations before the customer will feel comfortable deploying the device in production. It will be at that point that cash flow can turn positive.

Ultimately, said Liang, the United States needs to think about how to create a more vibrant ecosystem for startups so that more startups will generate more ideas and innovative products that can actually be deployed in the marketplace. The key will be to provide access to technology and fabs at a lower cost and decrease the timeline for generating revenues. In his opinion, it is imperative to figure out early if a potential chip has a market fit, and that will require alternative procurement processes that are more amenable to the timeframe on which startups need to operate.

To conclude his presentation, Liang described how SambaNova has gone about funding its development efforts. The company's technology came out of Stanford University, and he and his two Stanford co-founders secured research funding from the Defense Advanced Research Projects Agency (DARPA). They also collaborated with Department of Energy (DOE) national laboratories to deploy their product in a commercial manner, which allowed the company to lower some of its costs and speed integration of its product into the commercial space. Currently, 5-year-old SambaNova has raised over $1 billion and has some 500 employees, which Liang said may seem large for a startup but is what it takes to build a cutting-edge technology company.

In closing, Liang said that standards are important for allowing startups such as his company to use open-market technology and available IP. Also crucial is having access to cutting-edge fabs at a cost that is proportional to what a startup can afford, as well as having access to commercial endpoints to conduct a rapid test of market fit so that a company can show that it can stand on its own.

Aart DeGeus, Synopsys

Aart DeGeus said that semiconductors are at the center of the next evolution for humanity. From his perspective, the big opportunity today is to enable the scientific revolution needed to protect the planet, understand humanity and biology, and reset the infrastructure in which everyone connects. Chips are essential to this revolution because they are the computing engines, and they will have to be optimized for this task.

The semiconductor supply chain, said DeGeus, is simple to understand but complex to execute. It consists of design, followed by manufacturing, assembly, and testing, each step of which has deep disciplines supporting them. EDA has helped automate design and is supported by the use of big blocks of IP, which are pieces of design that can be reused for efficiency or for different situations. EDA is becoming even more relevant given the desire to develop new approaches on the computer rather than by experimenting in the fab, which is lengthy and expensive. It is also important, said DeGeus, for the software to align with the hardware on which it runs and to have the talent to conduct this work. He reiterated the previous speakers' calls for the nation to invest in talent development.

DeGeus said that in terms of market shares in different disciplines, the United States is in a strong position in the areas of EDA, IP, logic design, and manufacturing equipment. More investment is needed, however, in the area of materials, wafer fabrication, and assembly and testing. That said, U.S. investment in chip design is booming. Today, companies are investing more than 30 percent of annual revenues in EDA and IP research and development and around 18 percent of annual revenues in chip design, with those expenditures increasing by 15 percent from 2020 to 2021. This shows that companies are seeing the chance to invest for future opportunities.

DeGeus noted that there is a host of new entrants in the United States in terms of hyperscalers and device makers that now account for some 30 percent of overall chip design activity. As Liang mentioned, there has been a substantial increase in venture capital funding for semiconductors in the United States, a trend that is occurring in the rest of the world, too. In that respect, the race is on, said DeGeus, to further extend Moore's Law and to reach an inflection point to what he calls "SysMoore," which is systemic complexity but with a Moore's Law exponential ambition. This will require solving a set of problems that intersect many disciplines. Examples include using multi-die techniques that enable dramatically more transistors by using multiple chips and system optimization, which involves the intersection between software and hardware. To execute on this goal, his company is pledging to achieve a 1,000-fold increase in designer productivity, and realizing that pledge will require an immense amount of talent.

EDA innovations can drive engineer productivity, said DeGeus. AI-driven design, for example, has over the past two years produced superior design outcomes with a three- to five-fold improvement in the time it takes to achieve results. Investing in multi-die technology requires EDA given that success depends on how the multiple chips are connected, how different functions are split across two chips, and on avoiding

thermal issues. System virtualization, also called digital twinning, allows designers to build a model of how a chip will work before building the chip and to run software on chips that do not yet exist. Virtualization can also apply to manufacturing, said DeGeus, by creating the ability to model production processes to optimize capacity and yield for new technologies.

One interesting development, said DeGeus, is the availability of EDA as a service, which means that startups do not have to build an entire computer infrastructure and hire an information technology team. Rather, they can run EDA tools via the internet on a pay-per-use model. This software-as-a-service model could also provide the opportunity for large companies to run their task on hundreds of computers.

DeGeus said the federal government can help by first recognizing how strong the semiconductor industry is in the United States and then taking steps to protect it, protect innovation, and protect IP. The federal government should also ensure that U.S. companies have access to the global market to secure continued financing and to access the global talent pool. In terms of talent development, DeGeus recommended that a private-public partnership fund some 7,500 master's degrees per year for the next five years spread across perhaps 20 universities and some research hubs. He also recommended that international students receive a visa that will permit them to work in the United States, saying that it makes no sense to educate people and then send them away to become competitors in another country.

Another step DeGeus recommended was for the federal government to boost engineering skill development by having the most advanced tools and IP available for master's degree students to access. This will allow them to learn and practice designing with state-of-the-art tools. Finally, said DeGeus, the U.S. needs to reestablish itself as a magnet for talent. The U.S. university system is the best in the world, and attracting students should not be hampered by blocking the entry of international talent or restricting the number of green cards available. That must be separated from other immigration issues, said DeGeus. His final recommendation was for the federal government to orchestrate ecosystem-level innovation in areas such as next-generation multi-die architectures, ultra-low power applications, silicon photonics, and low-energy, high-performance computing.

National competitiveness is essential, said DeGeus, and so too is global leadership. To be sustainable, investments in semiconductors need to occur under an umbrella of something that is meaningful to mankind. As an analogy, he pointed to the 1960s effort to put a man on the moon as something that was seen as part of the future of humankind. The United States made a commitment and provided the funding to realize that goal, and it had an enormous impact, including the development of semiconductor technology. Today's mission, he suggested, should be to avoid climate catastrophe, something that will require semiconductors to enable the massive breakthroughs in science, technology, and engineering needed to reach zero carbon emissions by 2050.

John Neuffer, Semiconductor Industry Association

As the previous speakers noted, there are many challenges facing the semiconductor industry today, both short-term and long-term, said John Neuffer. Chief among them are the decline in onshore fabrication capacity, gaps and vulnerabilities in the supply chain that the COVID-19 pandemic has both accentuated and accelerated, challenges to U.S. technology leadership, weaknesses in key capabilities such as prototyping, and workforce deficiencies in terms of highly educated scientists and engineers as well as

technicians and construction workers. That said, the nation has a rare opportunity to address these challenges and pave the way for continued American leadership in chip innovation and manufacturing. The CHIPS Act, along with an investment tax credit provided by the Facilitating American-Built Semiconductors Act (FABS) Act, are critical pieces of the solution.

Neuffer noted that there is a pressing need for new manufacturing capacity at the leading and trailing edges of the pipeline. In the 1990s, the United States accounted for 37 percent of modern commercial chip capacity, but that is down to 12 percent today. The current chip shortage, triggered by weaknesses in the supply chain, has affected virtually all parts of the economy and the nation's defense-industrial base. If there is a silver lining to this situation, said Neuffer, it is that the pandemic and chip shortage have significantly increased awareness about the centrality of chips among both policymakers and the general public.

Regarding the workforce pipeline, Neuffer said that addressing the deficiencies has always been challenging and is projected to get more difficult. According to an analysis by his organization, the semiconductor industry will require 42,000 additional employees over the next five years and another 238,000 workers in adjacent and supporting sectors. Without action, said Neuffer, the semiconductor industry will not be in a position to grow and innovate in a manner that will ensure its global leadership. He pointed out that there is a virtuous cycle between research and development, workforce development, and innovation. Both public and private investments in research and development help create the programs in universities and research institutions that attract the talent that powers the ideas and innovation that are the lifeblood of the semiconductor industry. The industry's research commitments and ambitions have everything to do with its ability to develop talent.

Neuffer emphasized that the United States is not alone in wanting to support semiconductor manufacturing, design, and research. Other nations have already passed their own versions of the CHIPS Act. Bipartisan action is underway in both the U.S. House and Senate to address these challenges and provide new opportunities for U.S. technology competitiveness, and he said he is hopeful that funding will be on its way in the near future. He explained that funding in the CHIPS Act falls into two general categories: $39 billion in grants for manufacturing incentives to produce more chips in the United States, and $13 billion for research and development focused on the lab-to-fab technology transfer process.

Neuffer said that from a research and development perspective, the most critical part of the CHIPS Act is establishing NSTC and a packaging program. The greatest need these programs should address is bridging the lab-to-fab gap, sometimes called the "valley of death" problem. Currently, the United States is the global leader in early-stage research and development, supported by government funding agencies and the private sector, so the prototyping and piloting stages of technology development are where the majority of NSTC and packaging program activities should focus. Development is also needed across the full computational stack, which means the nation needs innovation in advanced materials and structures, novel device and circuits, architectures that leverage these advances, and software and algorithms that make use of the full set of computing innovations. Within these areas, research must address technologies for logic and memory, as well as for analog and radiofrequency electronics. Each of these subsectors, said Neuffer, are critical in different ways to the U.S. economy and national security.

Neuffer added that it is crucial to invest in advances in packaging and testing, particularly for heterogeneous integration for edge devices and cloud infrastructure, and in advanced testing capabilities

with increased automation and high-density, high-speed interconnects. Developing automated design tools for both chips and packaging will be essential to retain global semiconductor leadership, he added, noting that this is a big, complex ecosystem and all parts of it need attention and tending.

In offering suggestions for how to structure NSTC and the packaging program, Neuffer said governance must be led by industry to ensure there will be successful technology transfer to the commercial sector. In his view, NSTC and the packaging program should be closely aligned or combined entirely if permitted by the authorizing legislation. The needs of semiconductor manufacturing and packaging are too interconnected to be treated separately, said Neuffer. Funding should be carefully and thoughtfully balanced between standing up new infrastructure and upgrading existing infrastructure. He pointed out that there are great existing facilities that can and should be leveraged both to save costs and get these programs up and running quickly, with new facilities considered as warranted. In addition, there should be some degree of centralization in order for scaled piloting to be feasible, since too much diffusion of resources risks creating an anemic, meandering result.

Neuffer stressed the importance of effectively addressing collaboration. NSTC and the packaging program only make sense if there is substantial collaboration. The pipeline of early-stage technologies that will need NSTC and the packaging program to assist with scaling will come from research agencies and organizations such as NSF, DOE, DARPA, the Semiconductor Research Corporation, the Albany Nanotech Complex, national laboratories, and other federal research centers and universities. It will be important, he said, to orchestrate collaboration among these various stakeholders with industry, but the more important thing is to be ambitious and to focus on the targeted objective to help bridge the valley of death so that innovative technologies can more easily make their way to commercial relevance.

Neuffer said that there is a need for substantial international collaboration in parallel to these domestic efforts. Such collaboration should include non-U.S. companies from U.S. allies, as well as international partners and organizations such as the Interuniversity Microelectronics Centre, as a means of leveraging important innovation that is occurring overseas. To avoid redundancies and drive stronger innovation when determining priorities, NSTC's and the packaging program's investment should factor in investment made by other governments to boost research and development and improve the supply chain.

The CHIPS Act, said Neuffer, rests on two pillars: incentives for manufacturing and incentives for research. Both are needed, and the potential value of a successful NSTC and packaging program cannot be overstated. These programs will not only address the weakest links of the present semiconductor technology pipeline—crossing the valley of death and improving the nation's advanced packaging capabilities—but they will also serve as a major asset in workforce training and development. In closing, he underscored that this effort must place a significant focus on assisting semiconductor startups by providing much-needed capacity for prototyping and piloting of their innovative designs and technologies. In addition, he pointed out the FABS Act tax credit with a design component can be of great assistance to startups, which work almost entirely on the design side of the pipeline.

Zuber moderated the Q&A and discussion between PCAST Members and Gelsinger, Raina, Liang, DeGeus, and Neuffer.

PUBLIC COMMENT

Gregory Byrd, Global Coalition for Efficient Logistics provided two minutes of public comments.

CLOSING COMMENTS

The co-chairs expressed their appreciation to the speakers for their presentations and to PCAST members for their participation in these discussions that are so important for the future of our country.

MEETING ADJOURNED: 4:05 PM Eastern Time

I hereby certify that, to the best of my knowledge, the foregoing minutes are accurate and complete.

Frances Arnold, Ph.D.
Co-Chair
President's Council of Advisors on Science and Technology

Francis Collins, M.D., Ph.D.
Co-Chair
President's Council of Advisors on Science and Technology

Maria Zuber, Ph.D.
Co-Chair
President's Council of Advisors on Science and Technology