

Accelerating US Semiconductor Innovation

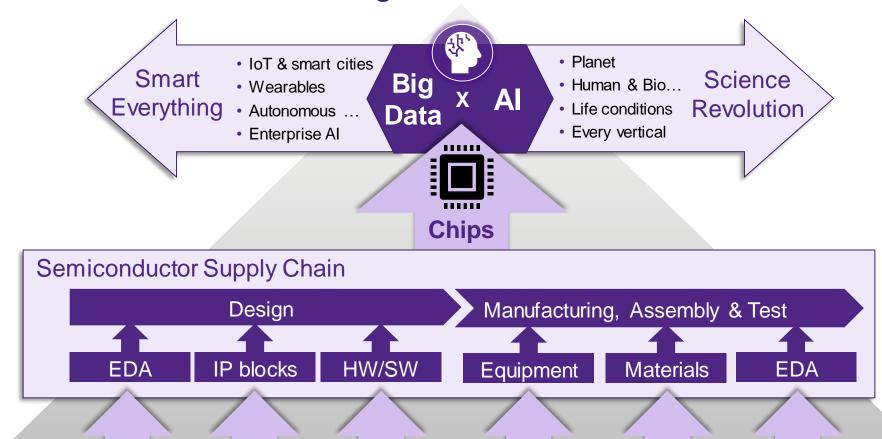
Opening remarks for PCAST meeting

Aart de Geus, Chairman and CEO Synopsys, Inc.

May 12, 2022

Semiconductors at Center of Competitiveness in 21st Century

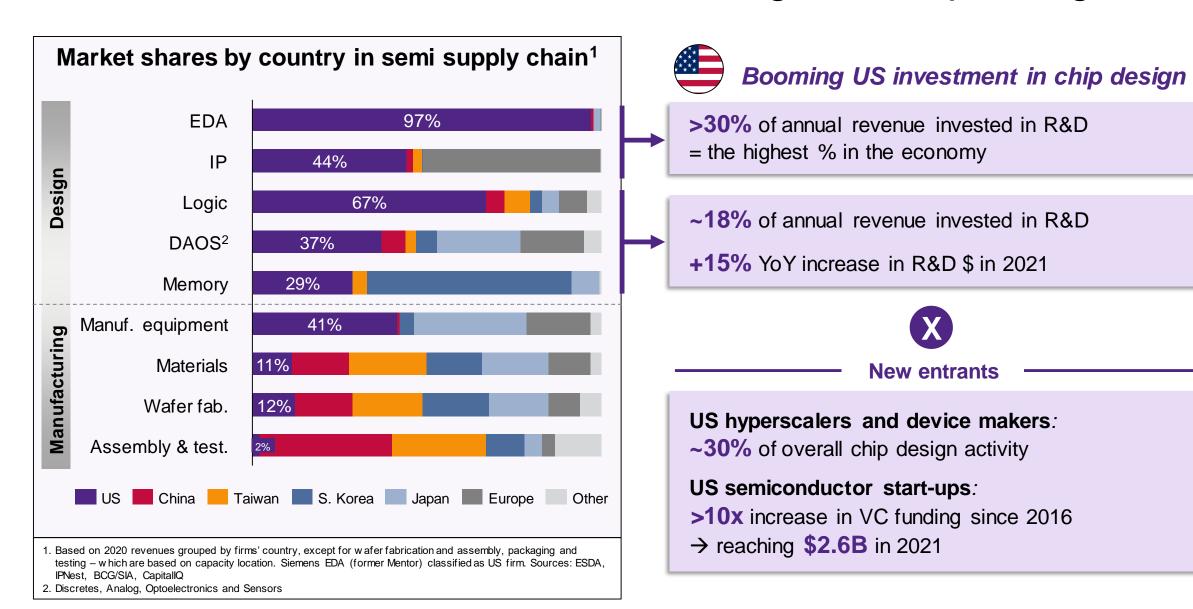
Progress of Mankind



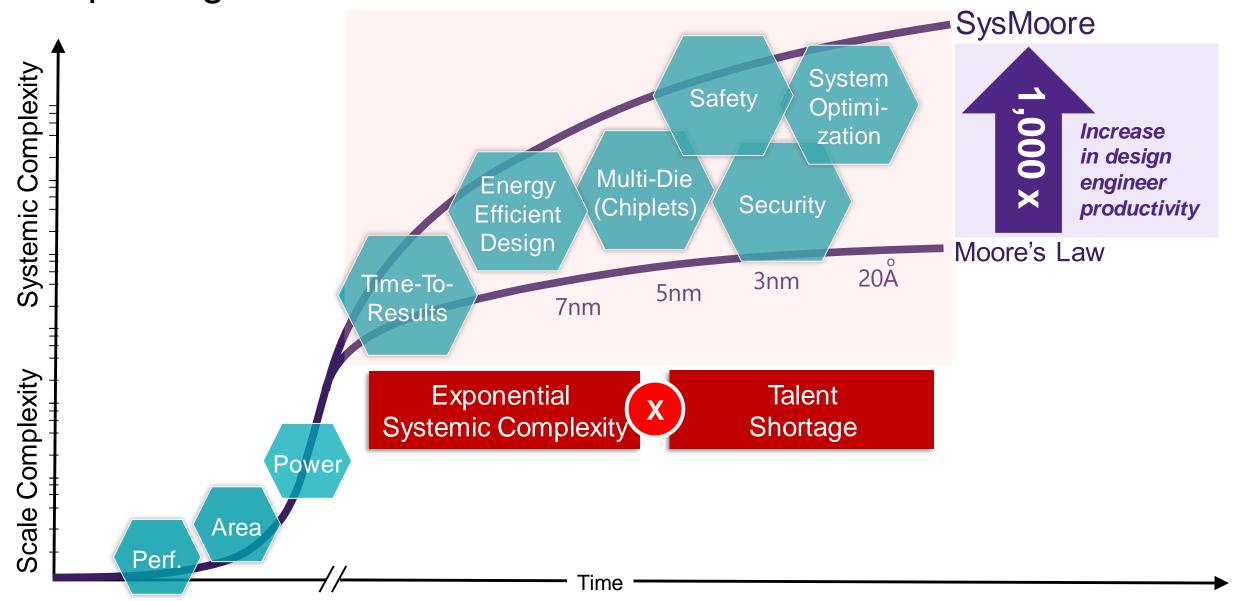
Human Talent

Shortage... Bright, diverse, innovative, competitive... & global!

US Can Build From a Position of Strength in Chip Design



Chip design innovation: the race is ON!



EDA Innovation Turbocharges Semicomductors

Al-Driven Design

✓ Superior design outcomes in much less time

Multi-Die (Chiplets)

✓ Many more transistors

- ✓ Better yield and production costs
- ✓ Test & re-use of "known good dies": the new IP

System Virtualization

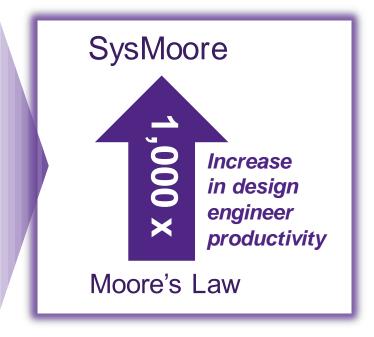
- ✓ Acceleration of SW development
- ✓ Digital twins for Silicon lifecycle management

Manufacturing Virtualization

- ✓ Technology (Classic & Multi-Die)
- ✓ Capacity (Classic & Multi-Die)

EDA SaaS

- ✓ Infinite elastic compute
- Immediate access without upfront IT investment
- ✓ Flexible, scalable "pay-as-you-use" licensing



Innovation

EDA

How can the US Government support the industry?

A) Protect US innovation model

 Private sector enterprise – with adequate incentives for R&D Access to global markets and global talent Intellectual Property (IP) rights



US policy in support of leadership in semiconductor design

B) Expand US chip design talent base

- 1 Fund 7,500 MS-graduates/year in semiconductors
 - US firms need +10% annual increase in design engineers
 - 20 universities, 2-year semiconductor funded Masters
 - \$120K/engineer → \$900M/year x 5 years → **\$4.5B**
 - Public-private funding for top students
 - Foreign talent: Visa + work-permit after graduation
- 2 Boost design engineering skill development
 - Access to state-of-the-art EDA + IP through universities and incubation centers → \$150-300M/year
- 3 Re-establish US as global talent magnet
 - Green card cap exemption for international advanced technical degree holders

C) Orchestrate ecosystem-level innovation

- 1 Next-generation multi-die (chiplet) architectures
 - Critical for HPC/AI roadmap
 - Exponential systemic complexity and connectivity
 - Requires standards/concerted effort across value chain
 - Linked to development of US adv. packaging capabilities
- 2 Other potential high-impact innovation areas
 - Ultra Low Power
 - High Performance Computing (HPC) power optimization
 - Silicon photonics
 - New materials: SiC (power), GaN (RF)

The new "great American enterprise"

May 25, 1961...

"Put a man on the Moon"





- a great new American enterprise, key to our future on Earth...
- f no project will be more important in the long-range; and none will be so difficult or expensive...
- this nation should commit to achieving the goal before this decade is out



- ~\$150B of funding over ~10 years
- Sparked development of many new technologies

Technology

- **Semiconductor** Apollo Guidance Computer first to use newly invented Integrated Circuits
 - Apollo was the world's largest customer for chips driving the growth of Silicon Valley

A mission that is meaningful to mankind



Avoid Climate Catastrophe

A new great American enterprise to avoid climate catastrophe...

- ... requiring massive breakthroughs in science, technology and engineering
 - → enabled by semiconductors!



Thank You

