# Accelerating Semiconductor Innovation in the U.S.

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## What are the largest challenges and opportunities for the U.S. semiconductor industry?

**U.S.'s strength** lies in its **ability to innovate**

Innovation in the semiconductor industry is being limited by **three key challenges**

- Ending of Moore's law
- Enormous complexity of designing hardware-software systems
- Declining student interest in semiconductor design

# There is an opportunity for a dramatic reinvention of system design

Similar to the 1980s when chip design moved from a few large companies with in-house fabs to many small fabless ones

Enabled by **electronic design automation** (EDA) tools that greatly **simplified chip design**

Made chip design ***accessible to a larger set of people***, allowing them to **innovate**

# Critical areas of research in semiconductor design

**Domain-specific hardware accelerators** promising for continued performance scaling in the post Moore era

- Key **driver** for **large-scale deployment** of machine learning, image processing, video coding, cryptography
- But **incur large** design, verification and software engineering **costs**

**Cost: Software Stack > Verification > Design > Prototype**

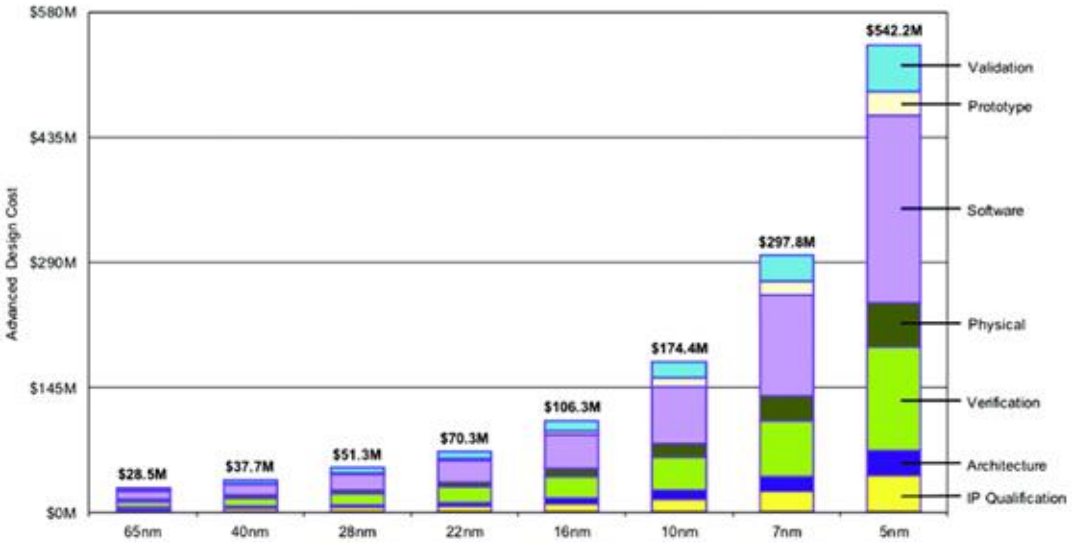



Figure source: Chiplet Heterogeneous Integration Technology—Status and Challenges - Scientific Figure on ResearchGate. Available from: https://www.researchgate.net/figure/Chip-Design-and-Manufacturing-Cost-under-Different-Process-Nodes-Data-Source-from-IBS_fig1_340843129 [accessed 11 May, 2022]

# Critical areas of research in semiconductor design

Research on tools to reduce the cost of design, verification and deployment of end-to-end systems with domain-specific accelerators

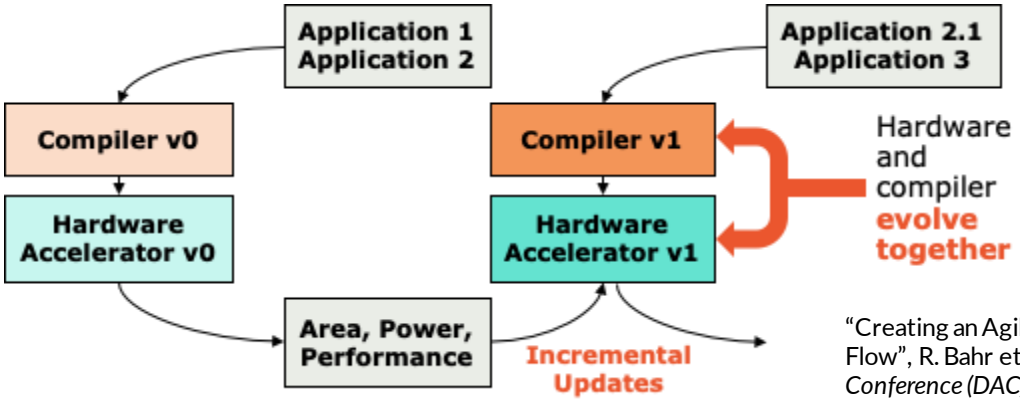
**Methodologies that raise the level of abstraction for design and verification of hardware/software systems**

**Automated co-design of programmable accelerators and compilers for fast-changing application domains**

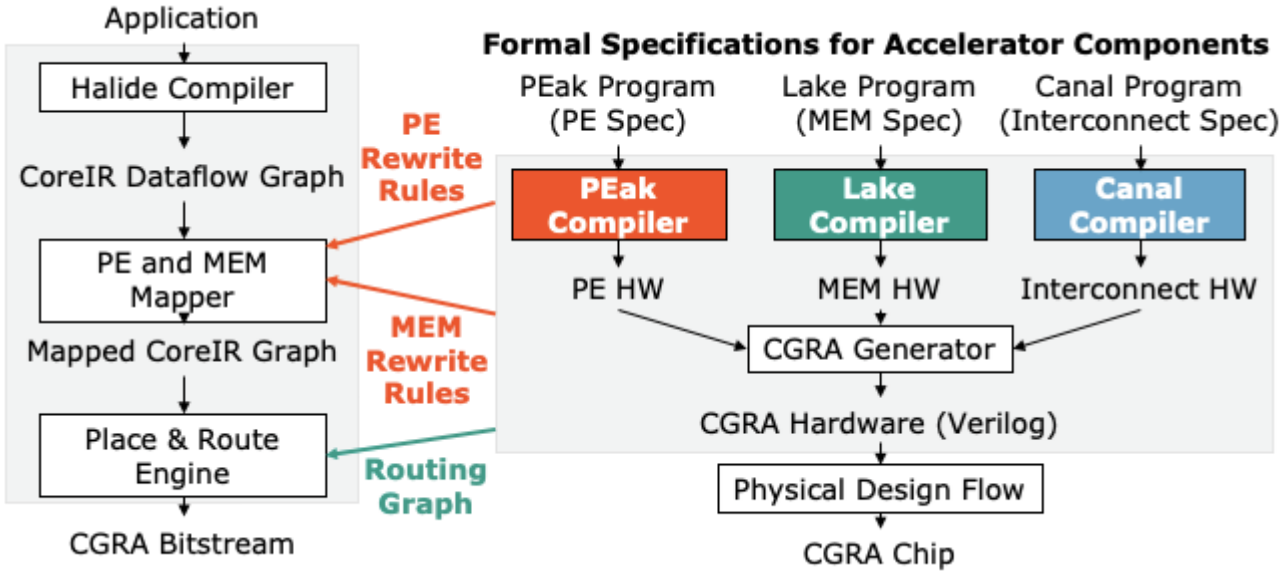
**Tools for automated design space exploration and optimization**

# Agile Hardware Software Co-design

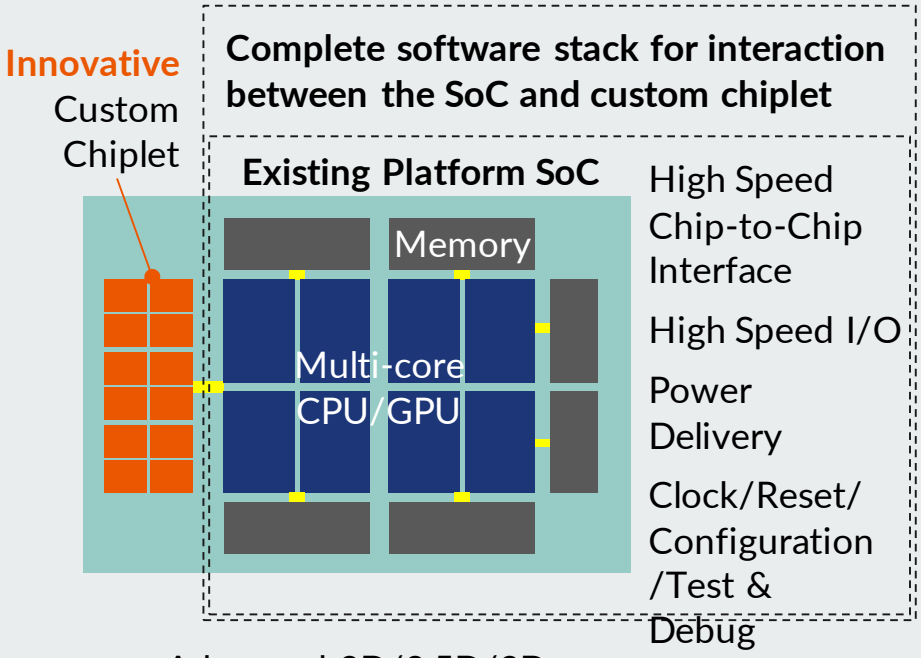
Automatic generation of hardware accelerator and compiler collateral from a single specification




"Creating an Agile Hardware Design Flow", R. Bahr et al, *Design Automation Conference (DAC)*, July 2020.



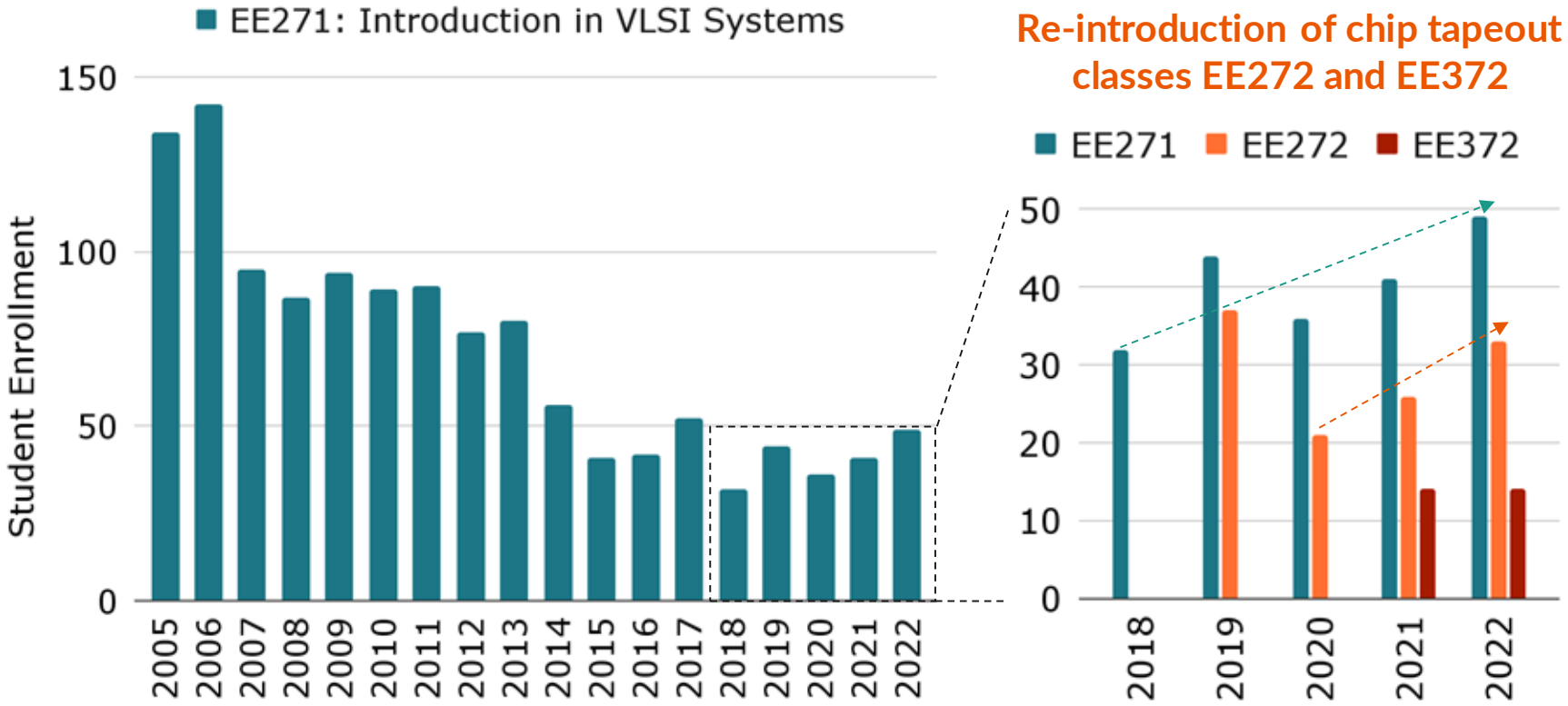
# How would you reduce the barriers to entry for semiconductor startups?




- Semiconductor startups spend a large fraction of design time and investment on **non-innovative portions** of the design, which are **too complex to build from scratch, or by putting together IP**
- To reduce time to market, we need to create a ***chiplet* ecosystem**, which **provides a platform SoC (+ software stack)**, to which **innovative chiplets can attach**
- Will usher in a new wave of system innovation!

## How do we attract more skilled workers / students to the semiconductor industry?

- Students are drawn to areas that capture their interest and imagination
- To capture interest, it is important to empower small groups to innovate and create exciting systems
- This is not possible with today's chip design approach, and thus interest in this area has been declining for many years, and students have moved towards computer science




**Student enrollment in graduate-level chip design classes at Stanford University**

exciting

# What is needed to teach ~~more~~ chip design courses at U.S. universities?

Reinvigorate student interest by supporting prototyping of student-designed chips by giving access to

- Multi-project wafer fabrication runs through a MOSIS-like aggregator
- Industry-standard EDA tools ✓
- Computing infrastructure ✓

Fund universities to develop, maintain and freely share chip design flows and libraries

Chip layouts of student designs prototyped in EE372, Spring 2021

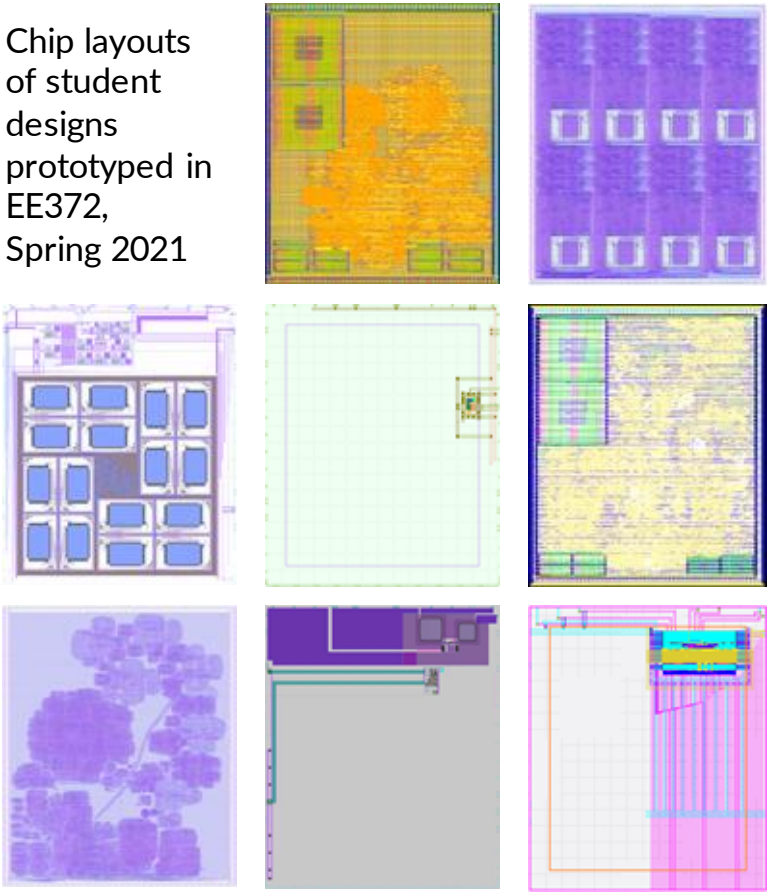


Figure source: https://priyanka-raina.github.io/ee272b-spring2021/

# What would you like to see from a National Semiconductor Technology Center (NSTC)?

1. Support research on tools to dramatically reduce for the cost of design, verification and deployment of systems with domain-specific accelerators

2. Create a chiplet ecosystem, which provides a platform SoC (+ software stack), to which innovative chiplets can attach using advanced packaging

3. Reinvigorate student interest in semiconductors by supporting chip design and prototyping classes